

# Compal Confidential

## PEW76/86/96 M/B Schematics Document

AMD Danube Only UMA

AMD Champlain Processor with RS880M/SB820M

2010-07-20

LA6552P REV: 1.0

|   |            |                    |            |                          |         |
|---|------------|--------------------|------------|--------------------------|---------|
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| Date: Thursday, July 22, 2010   |            |                    |            | Sheet                    | 1 of 45 |

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Model Name : PEW96

File Name : LA-6552P

P/N : DA60000IM10

PCB

ZZZ

LA-6552P RE1 MB

LA-6552P MB Rev0: DA60000IM00

LA-6552P MB Rev1: DA60000IM10

LA-6552P MB Rev1: DAZ0FQ00200

Danube

AMD SIG4 Processor

uPGA-638 Package

Champlain page 6,7,8,9

Memory BUS(DDR3)

Dual Channel

1.5V DDRIII 1066~1333MHz

204pin DDRIII-SO-DIMM X2

BANK 0, 1, 2, 3

page 10,11

Hyper Transport Link

16 x 16

ATI RS880M

uFCBGA-528

page 12,13,14

A link Express2

Gen1

ATI SB820M

uFCBGA-605

page 18,19,20,21,22

Thermal Sensor

ADM1032

page 8

LVDS

page 15

CRT

page 17

HDMI Conn.

page 16

MINI Card 1

WLAN

page 26

GPPI

LAN(GbE)

Broadcom

BCM57780

page 24

GPP0

RJ45

page 25

LED

page 29

Fan Control

page 32

RTC CKT.

page 18

LID SW / MEDIA/B

page 28

Power On/Off CKT.

page 32

DC/DC Interface CKT.

page 33

Power Circuit

page 34,35,36,37,38  
39,40,41,42

Extend Card/B

1. USB X2

2. ODD X1

Touch Pad

page 29

Int.KBD

page 29

EC I/O Buffer

page 29

BIOS

page 29

LPC BUS

ENE KB926

page 28

SATA HDD

Conn. page 23

port 0

SATA ODD

FFC Conn. page 23

port 1

S-ATA

Gen2

3.3V 48MHz

3.3V 24.576MHz/48Mhz

HD Audio

HDA Codec

ALC272X

page 30

Audio AMP

page 31

Phone Jack x2

page 31

|   |                    |                 |            |                               |               |
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| Power Plane  | Description                                     | S1  | S3  | S5  |
|--------------|---|-----|-----|-----|
| VIN          | Adapter power supply (19V)                      | N/A | N/A | N/A |
| B+           | AC or battery power rail for power circuit.     | N/A | N/A | N/A |
| +CPU_CORE    | Core voltage for CPU (1.375-1.5V)               | ON  | OFF | OFF |
| +CPU_CORE_NB | Voltage for On-die Northbridge of CPU(0.8-1.1V) | ON  | OFF | OFF |
| +CPU_VDDR    | 1.05V switched power rail                       | ON  | OFF | OFF |
| +0.75V       | 0.75V switched power rail for DDR terminator    | ON  | ON  | OFF |
| +1.1VS       | 1.1V switched power rail for NB VDDC & VGA      | ON  | OFF | OFF |
| +1.5V        | 1.5V power rail for CPU VDDIO and DDR           | ON  | ON  | OFF |
| +1.5VS       | 1.5V power rail for MINI Card                   | ON  | OFF | OFF |
| +1.8VS       | 1.8V switched power rail                        | ON  | OFF | OFF |
| +2.5VS       | 2.5V for CPU_VDDA                               | ON  | OFF | OFF |
| +3VALW       | 3.3V always on power rail                       | ON  | ON  | ON* |
| +3VS         | 3.3V switched power rail                        | ON  | OFF | OFF |
| +3V_LAN      | 3.3V power rail for LAN                         | ON  | ON  | ON  |
| +5VALW       | 5V always on power rail                         | ON  | ON  | ON* |
| +5VS         | 5V switched power rail                          | ON  | OFF | OFF |
| +VSB         | VSB always on power rail                        | ON  | ON  | ON* |
| +RTCVCC      | RTC power                                       | ON  | ON  | ON  |
|              |   |     |     |     |
|              |   |     |     |     |

## External PCI Devices

**EC SM Bus1 address**

**EC SM Bus2 address**

**SB820**  
**SM Bus 0 address**

| Device                             | Address    | HEX | Device | Address |
|------------------------------------|------------|-----|--------|---------|
| Clock Generator (SILEGO SLG8SP626) | 1101 001Xb | D2  |        |         |
| DDR DIMM1                          | 1001 000Xb | 90  |        |         |
| DDR DIMM2                          | 1001 010Xb | 94  |        |         |
| Mini card                          |            |     |        |         |

**SB820**  
**SM Bus 1 address**

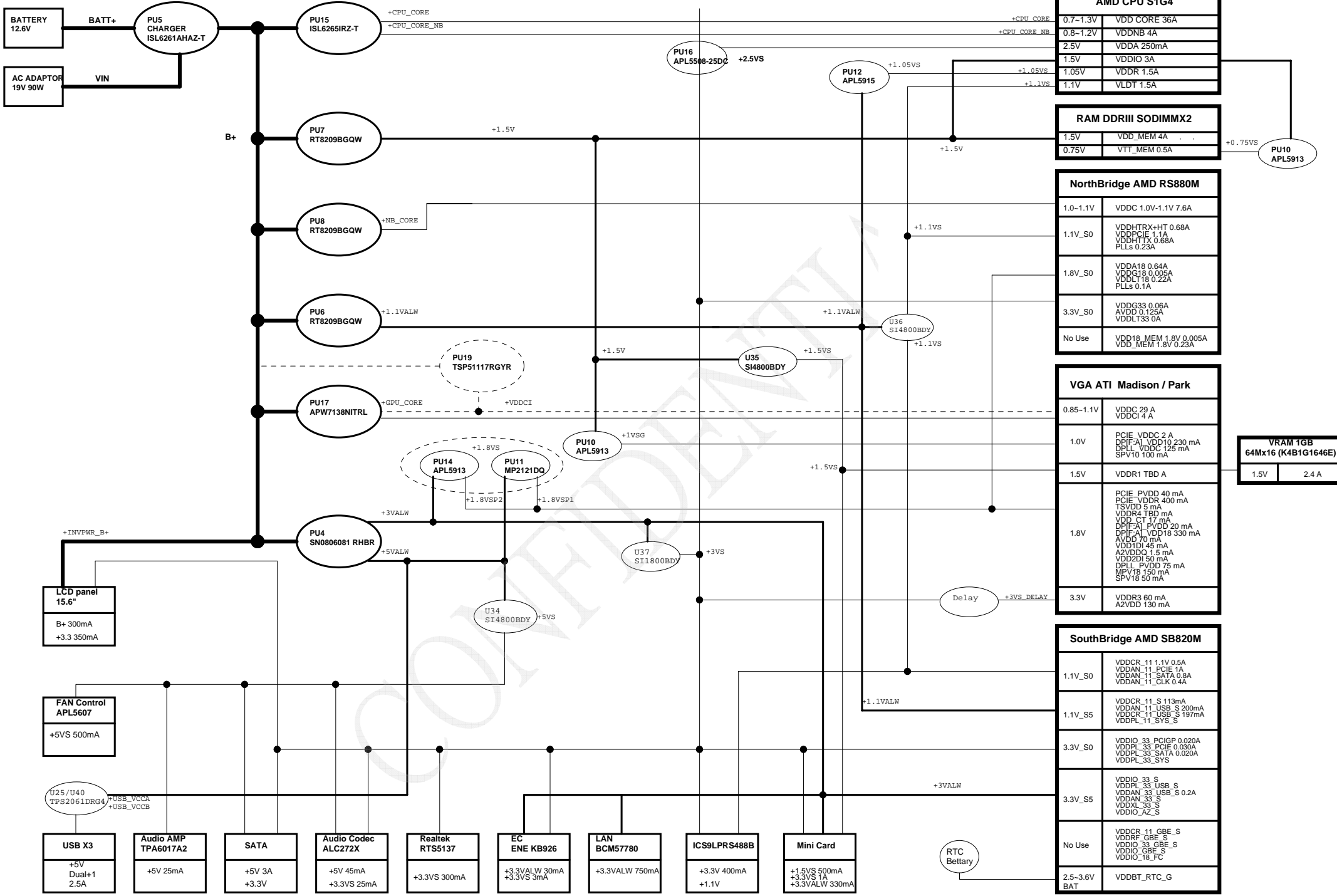
| STATE \ SIGNAL        | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V  | +VS | Clock |
|-----------------------|---------|---------|---------|---------|-------|-----|-----|-------|
| Full ON               | HIGH    | HIGH    | HIGH    | HIGH    | ON    | ON  | ON  | ON    |
| S1 (Power On Suspend) | LOW     | HIGH    | HIGH    | HIGH    | ON    | ON  | ON  | LOW   |
| S3 (Suspend to RAM)   | LOW     | LOW     | HIGH    | HIGH    | ON    | ON  | OFF | OFF   |
| S4 (Suspend to Disk)  | LOW     | LOW     | LOW     | HIGH    | ON    | OFF | OFF | OFF   |
| S5 (Soft OFF)         | LOW     | LOW     | LOW     | LOW     | ON    | OFF | OFF | OFF   |

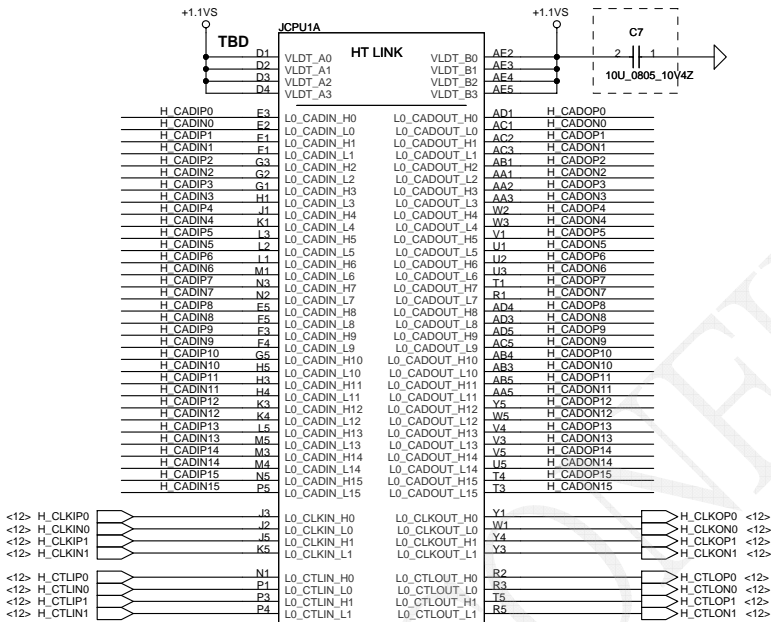
|          |              |             |             |             |
|----------|--------------|-------------|-------------|-------------|
| Vcc      | 3.3V +/- 5%  |             |             |             |
| Ra/Rc/Re | 100K +/- 5%  |             |             |             |
| Board ID | Rb / Rd / Rf | VAD_BID min | VAD_BID typ | VAD_BID max |
| 0        | 0            | 0 V         | 0 V         | 0 V         |
| 1        | 8.2K +/- 5%  | 0.216 V     | 0.250 V     | 0.289 V     |
| 2        | 18K +/- 5%   | 0.436 V     | 0.503 V     | 0.538 V     |
| 3        | 33K +/- 5%   | 0.712 V     | 0.819 V     | 0.875 V     |
| 4        | 56K +/- 5%   | 1.036 V     | 1.185 V     | 1.264 V     |
| 5        | 100K +/- 5%  | 1.453 V     | 1.650 V     | 1.759 V     |
| 6        | 200K +/- 5%  | 1.935 V     | 2.200 V     | 2.341 V     |
| 7        | NC           | 2.500 V     | 3.300 V     | 3.300 V     |

| Board ID | PCB Revision                          |
|----------|---------------------------------------|
| 0        | <i>EVT / PVT stage (w/ pach code)</i> |
| 1        |                                       |
| 2        |                                       |
| 3        |                                       |
| 4        |                                       |
| 5        |                                       |
| 6        |                                       |
| 7        |                                       |

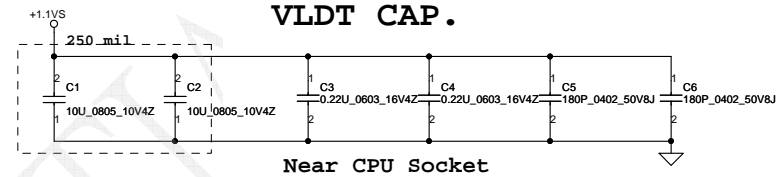
| Board ID | PCB Revision |
|----------|--------------|
| 0        |              |
| 1        | PEW76/86/96  |
| 2        |              |
| 3        |              |
| 4        |              |
| 5        |              |
| 6        |              |
| 7        |              |

[illegible]



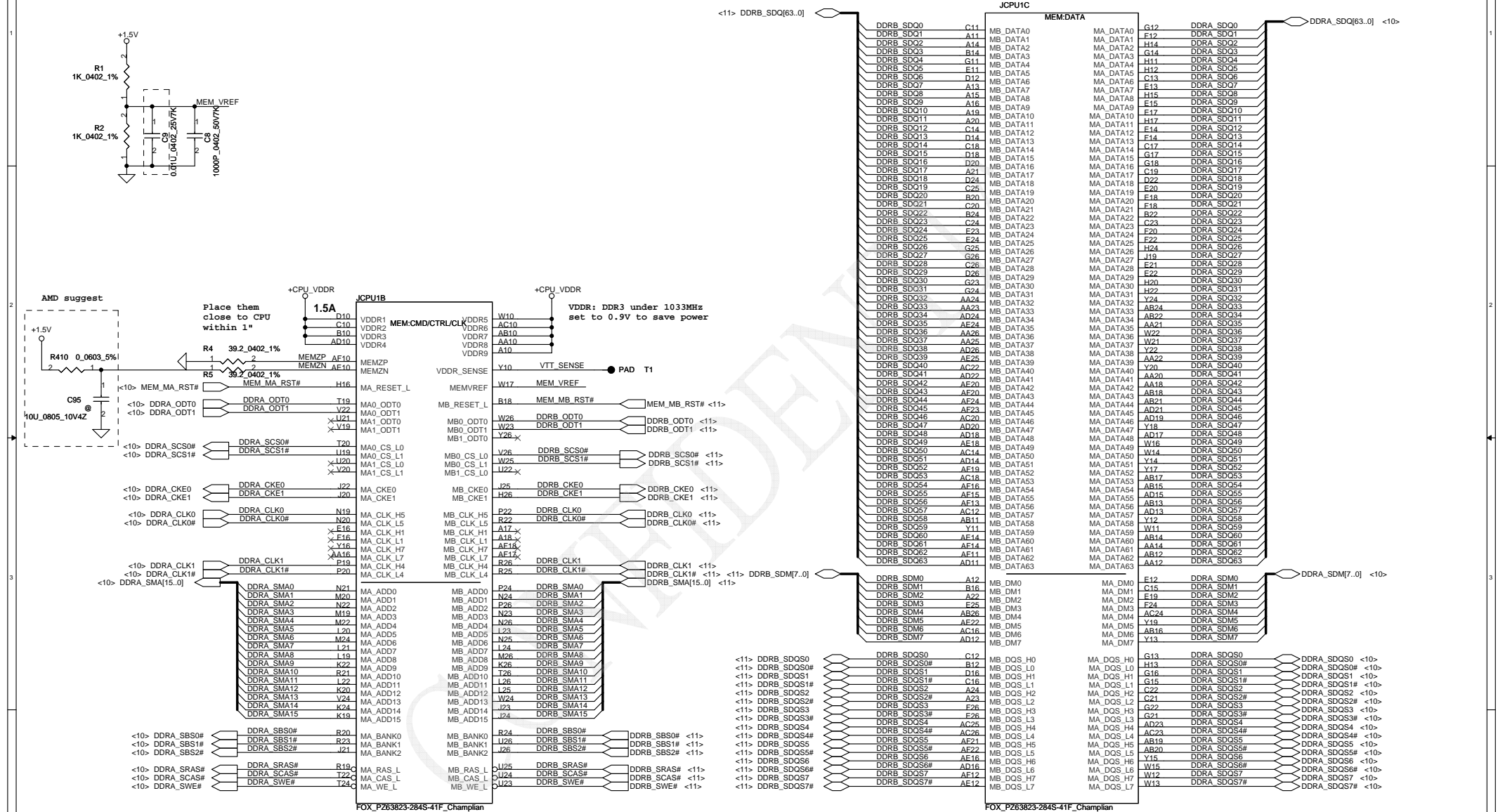


FOX\_P263823-284S-41F\_Champian



|   |            |                    |            |                          |         |
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## Processor DDR3 Memory Interface

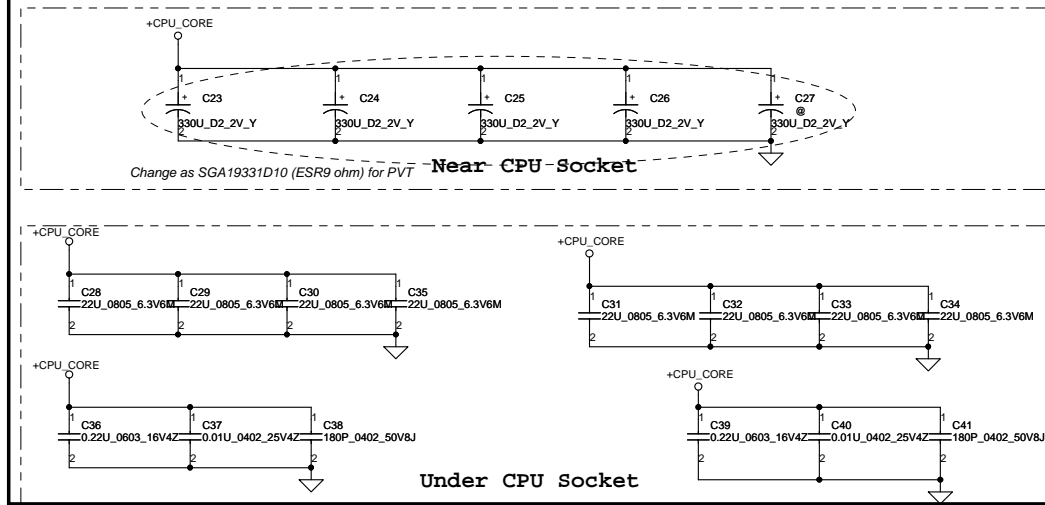


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|   |  |                    |  | AMD CPU S1G4 DDRIII I/F                  |  |                         |  |
|   |  |                    |  | Document Number<br>PEW/76/86/96 LA-6552P |  |                         |  |
|   |  |                    |  | Date                                     |  | Thursday, July 22, 2010 |  |
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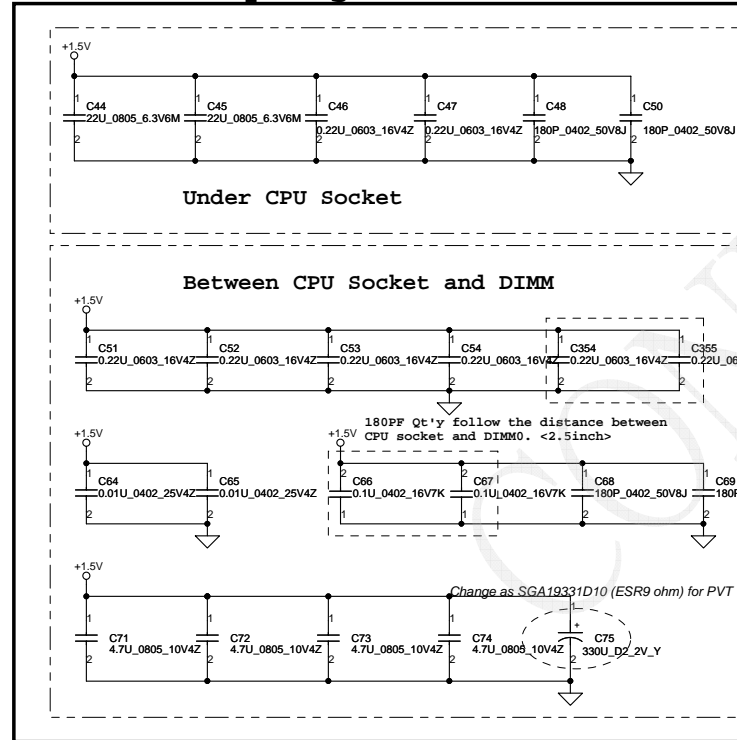




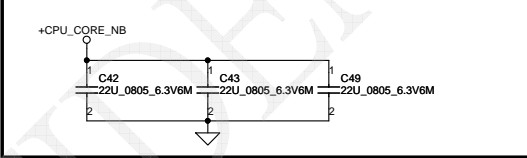
## VDD(+CPU\_CORE) decoupling.



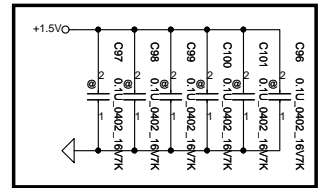
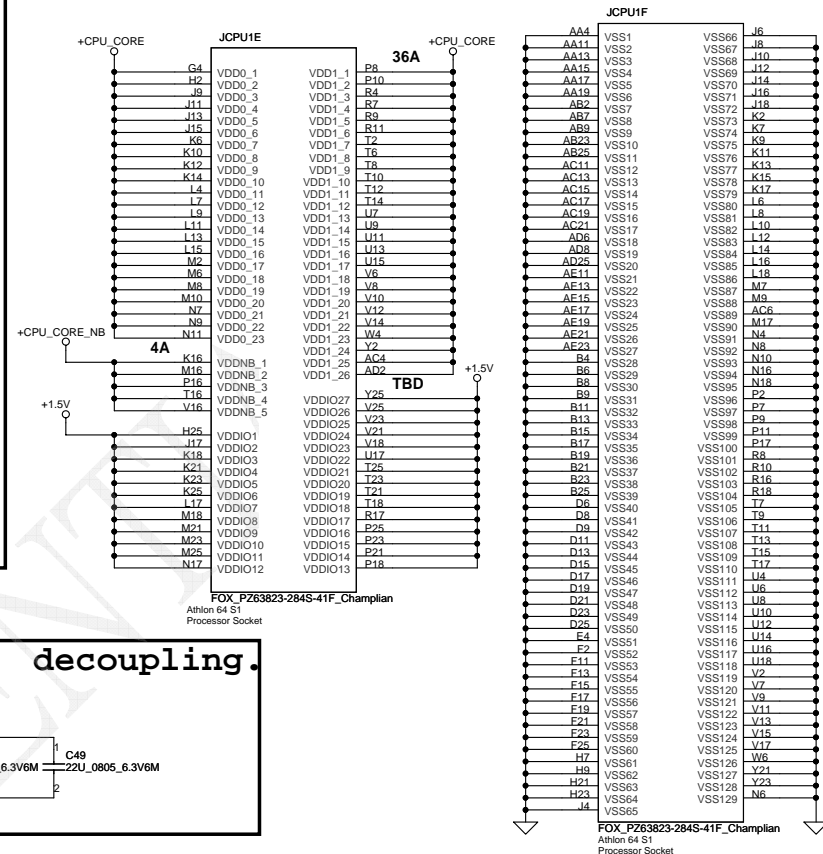
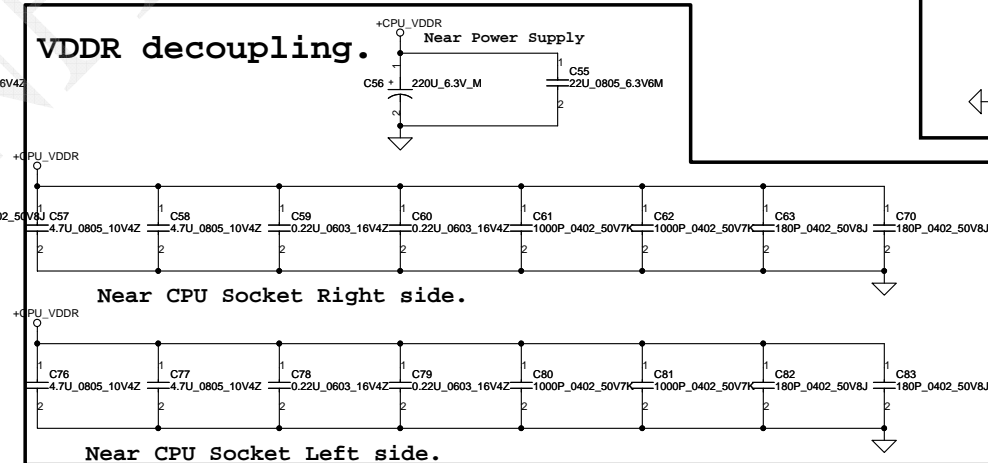
## VDDIO decoupling.



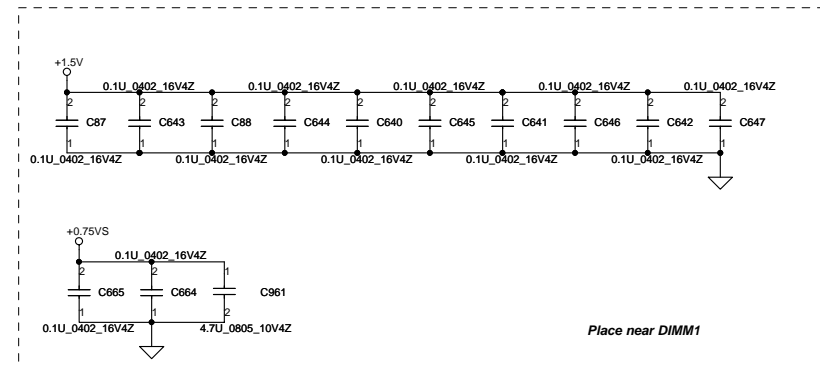
## +CPU\_CORE\_NB decoupling.



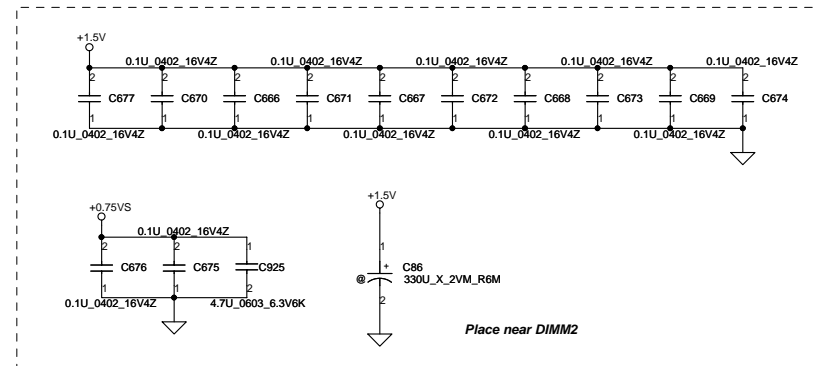
## VDDR decoupling.



|   |                         |                 |            |                 |                          |  |
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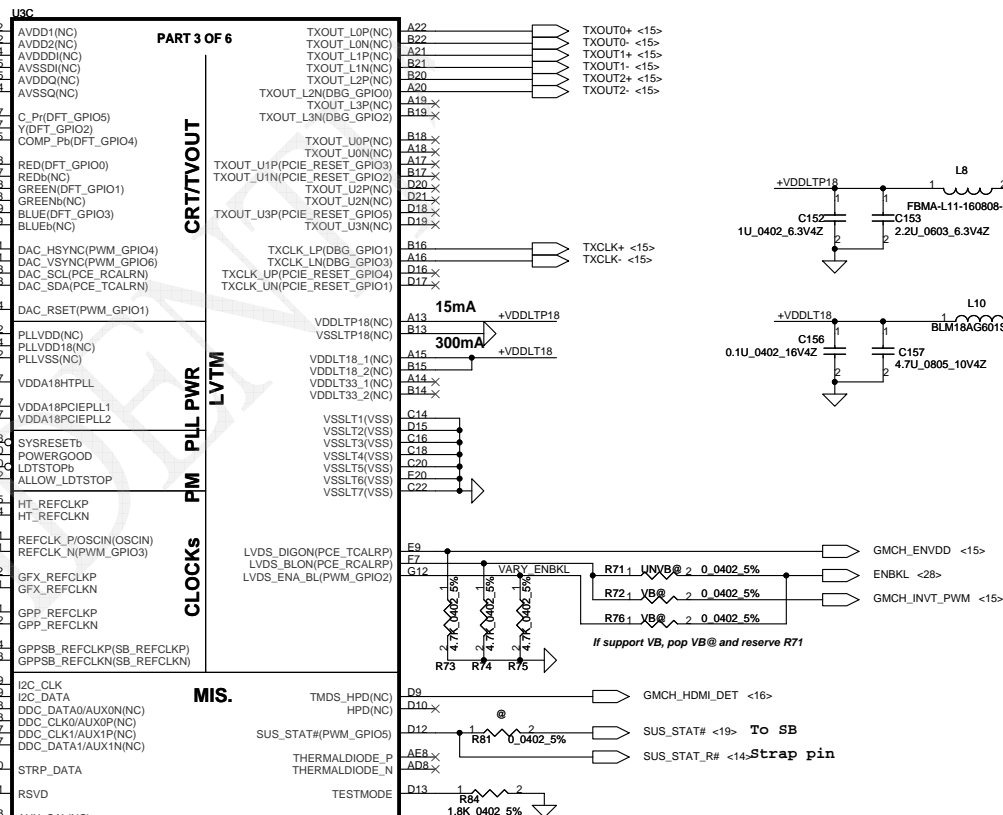
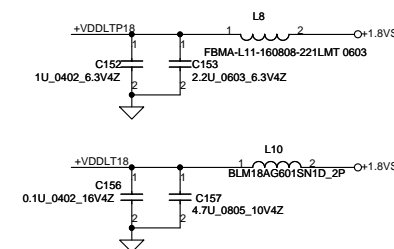
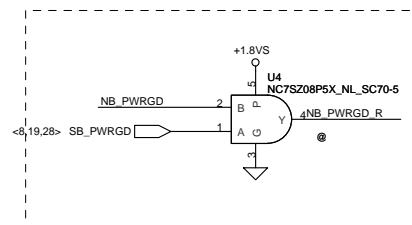
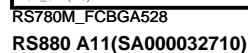
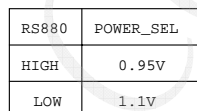
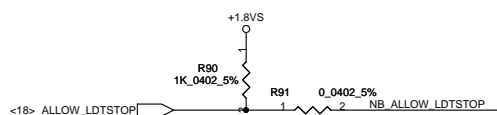
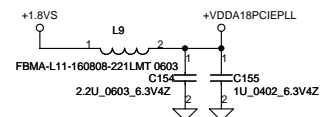


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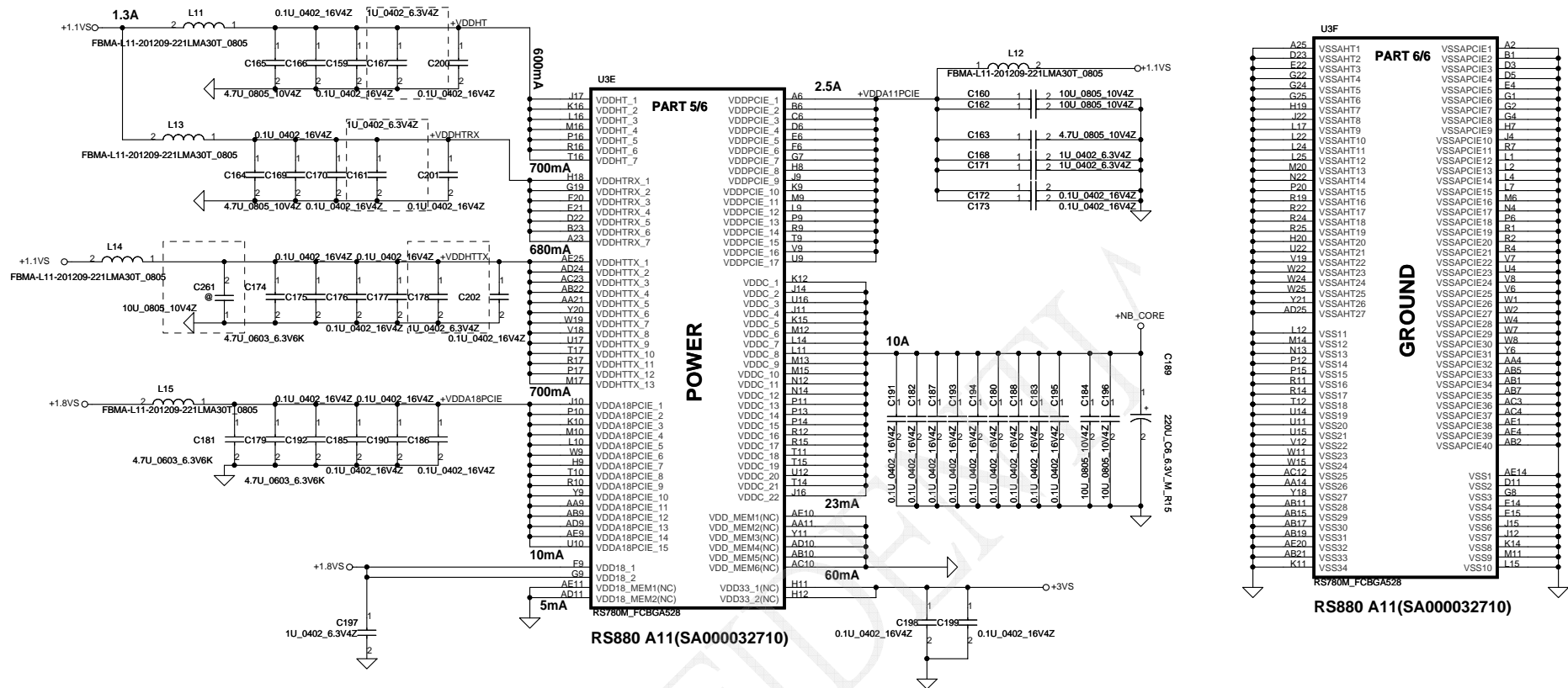


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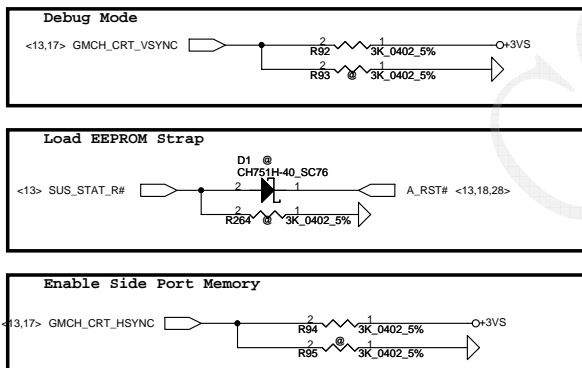




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|   |            |                    |            | Date: Thursday, July 22, 2010 | Sheet 13 of 45      |



## Side port and Strap setting



### DFT\_GPIO5:STRAP\_DEBUG\_BUS\_GPIO\_ENABLEB

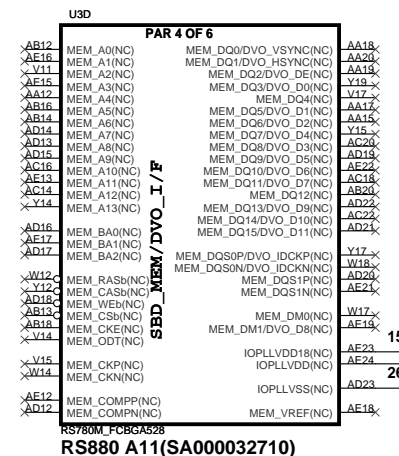
Enables the Test Debug Bus using GPIO. (VSYNC)  
1 : Disable  
0 : Enable

### DFT\_GPIO1: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM  
1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

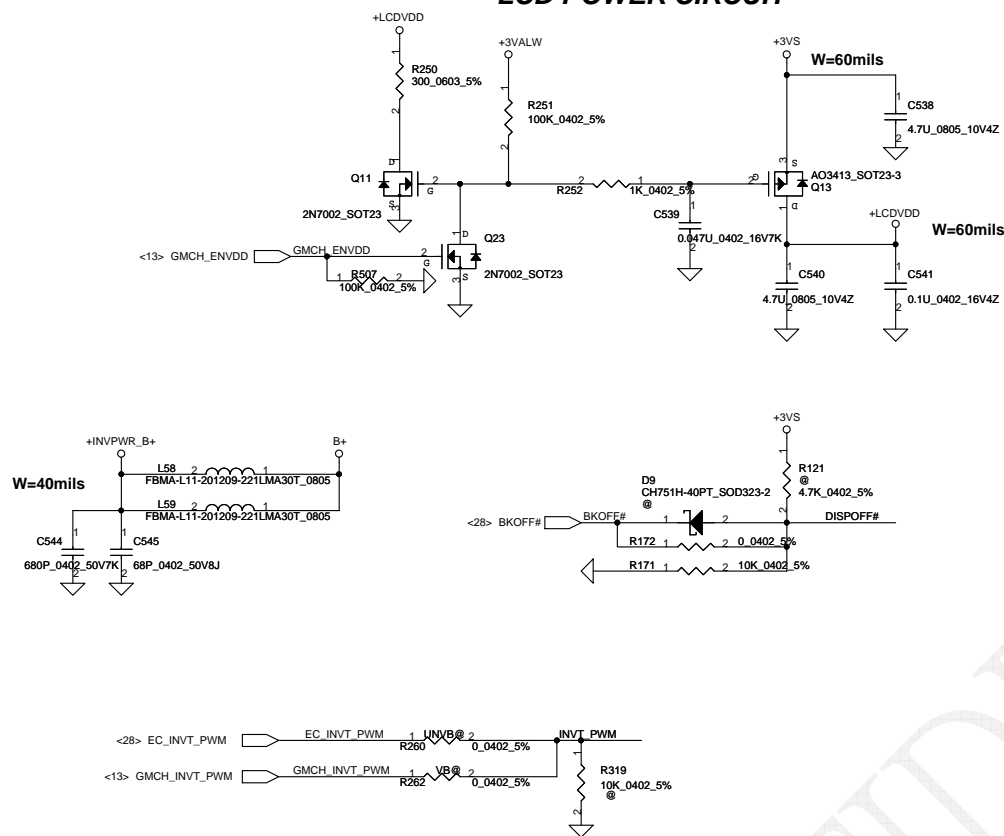
### Enable Side Port Memory

RS880: HSYNC#  
0 : Enable  
1 : Disable  
Register Readback of strap:  
NB\_CLKCFG:CLK\_TOP\_SPARE\_D[1]

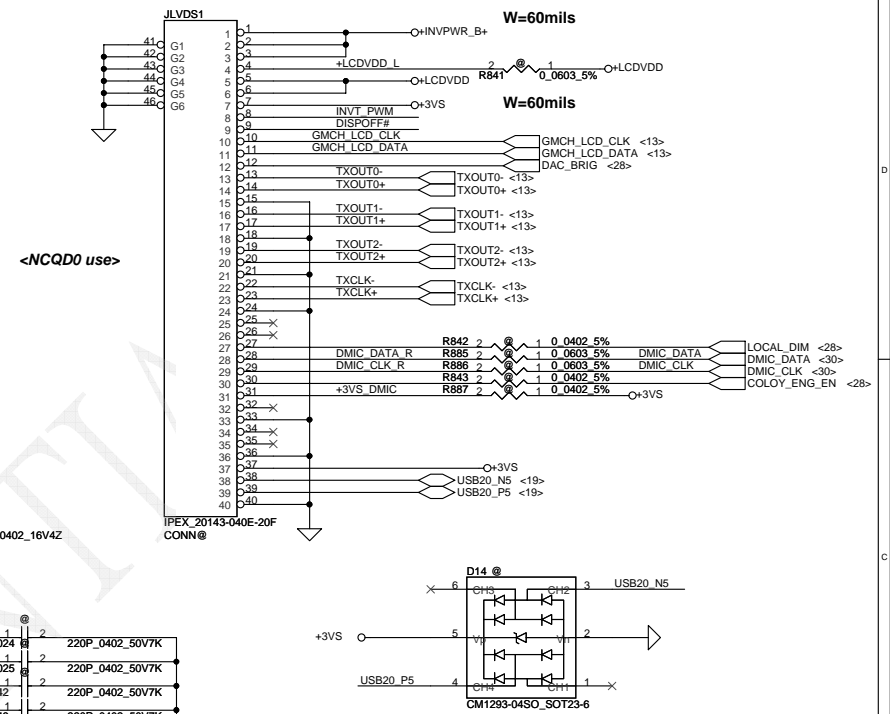


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| Date: Thursday, July 22, 2010  |            |                    |            | Sheet 14 of 45           |  |

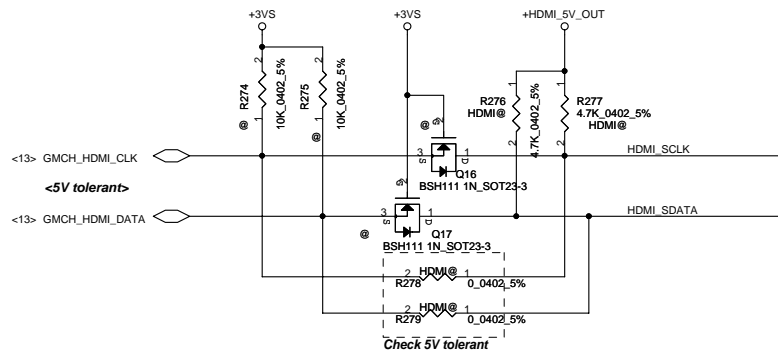
# LCD POWER CIRCUIT



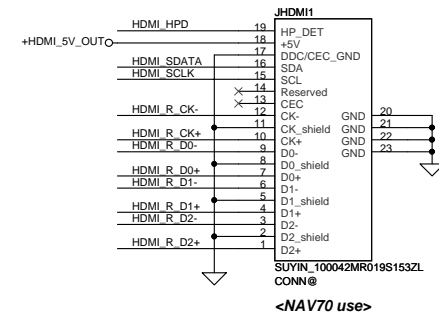
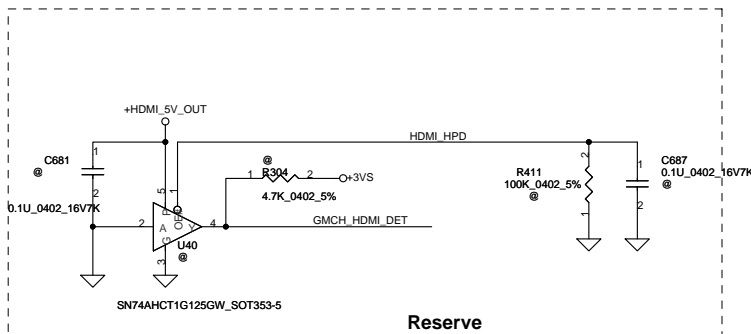
# LCD/LED PANEL Conn.



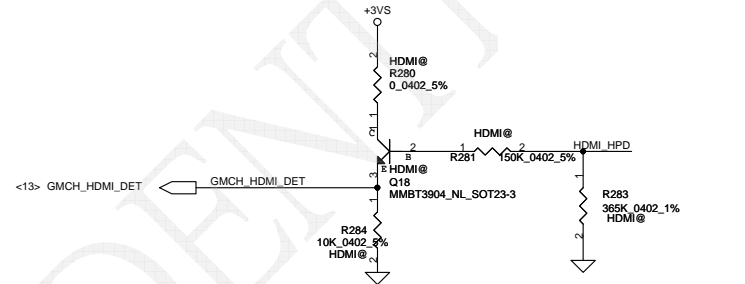
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|   |            |                    |            | Date: Thursday, July 22, 2010 | Sheet 15 of 45 |



Place closed to JHDMI1



<NAV70 use>

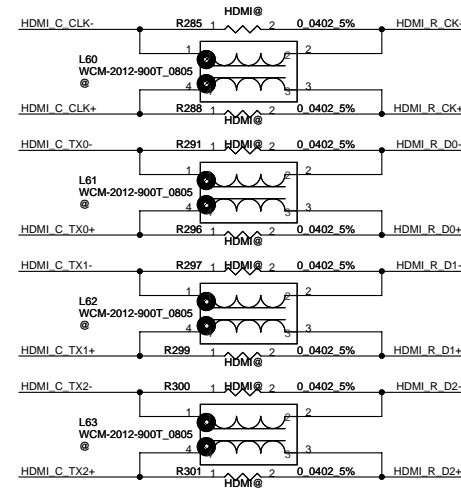


|                      |      |       |   |                 |             |      |   |       |   |             |
|----------------------|------|-------|---|-----------------|-------------|------|---|-------|---|-------------|
| <12> GMCH_HDMI_TXD2- | C550 | HDMI@ | 1 | 0.1U_0402_16V7K | HDMI C TX2- | R286 | 1 | HDMI@ | 2 | 715_0402_1% |
| <12> GMCH_HDMI_TXD2+ | C551 | HDMI@ | 1 | 0.1U_0402_16V7K | HDMI C TX2+ | R287 | 1 | HDMI@ | 2 | 715_0402_1% |
| <12> GMCH_HDMI_TXD1- | C552 | HDMI@ | 1 | 0.1U_0402_16V7K | HDMI C TX1- | R289 | 1 | HDMI@ | 2 | 715_0402_1% |
| <12> GMCH_HDMI_TXD1+ | C553 | HDMI@ | 1 | 0.1U_0402_16V7K | HDMI C TX1+ | R290 | 1 | HDMI@ | 2 | 715_0402_1% |
| <12> GMCH_HDMI_TXD0- | C554 | HDMI@ | 1 | 0.1U_0402_16V7K | HDMI C TX0- | R292 | 1 | HDMI@ | 2 | 715_0402_1% |
| <12> GMCH_HDMI_TXD0+ | C555 | HDMI@ | 1 | 0.1U_0402_16V7K | HDMI C TX0+ | R293 | 1 | HDMI@ | 2 | 715_0402_1% |
| <12> GMCH_HDMI_TXC-  | C556 | HDMI@ | 1 | 0.1U_0402_16V7K | HDMI C CLK- | R294 | 1 | HDMI@ | 2 | 715_0402_1% |
| <12> GMCH_HDMI_TXC+  | C557 | HDMI@ | 1 | 0.1U_0402_16V7K | HDMI C CLK+ | R295 | 1 | HDMI@ | 2 | 715_0402_1% |

UMA 715 ohm



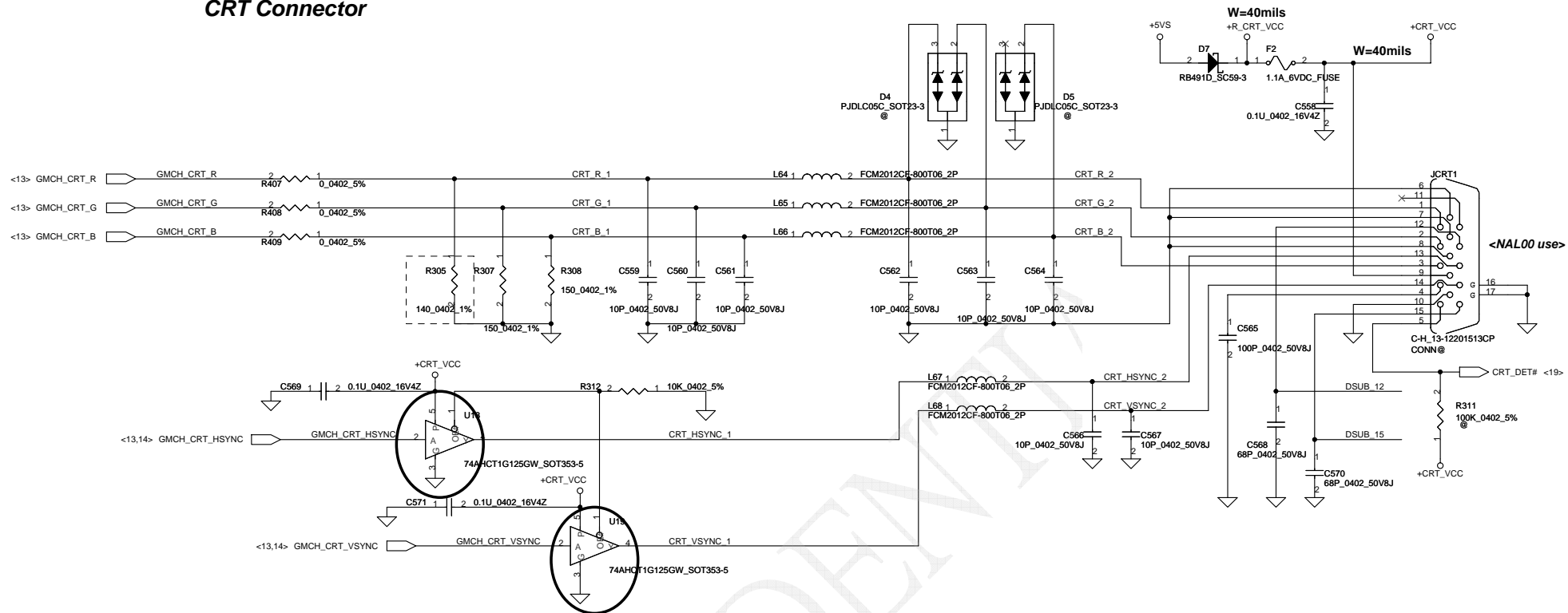
Place closed to JHDMI1



|   |                    |                               |                |
|---|--------------------|-------------------------------|----------------|
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|   |                    | PEW76/86/96 LA-6552P          |                |
|   |                    | Date: Thursday, July 22, 2010 | Sheet 16 of 45 |

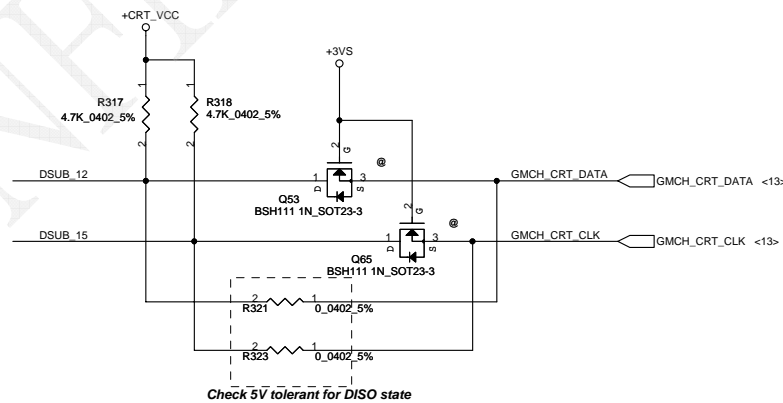


# CRT Connector

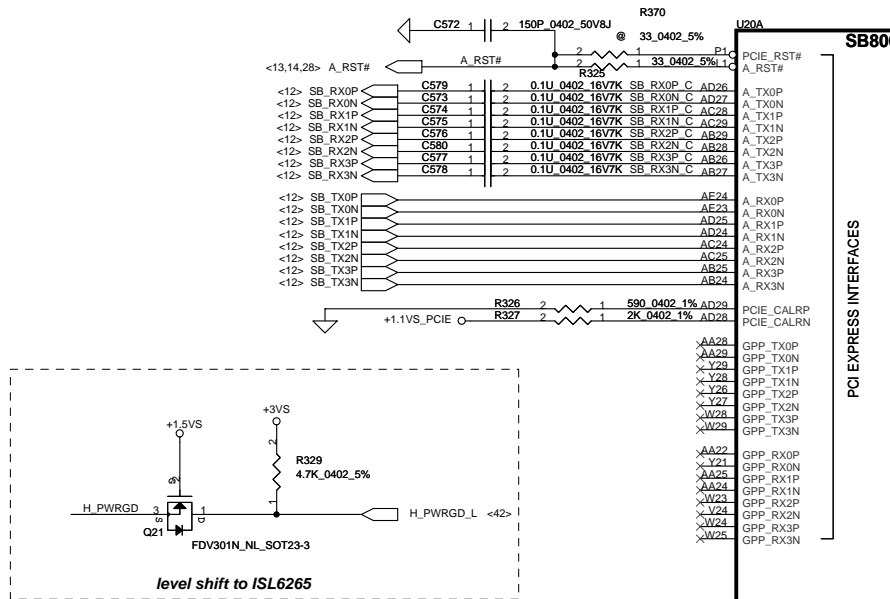


Change as SA411250110

Close to Conn side

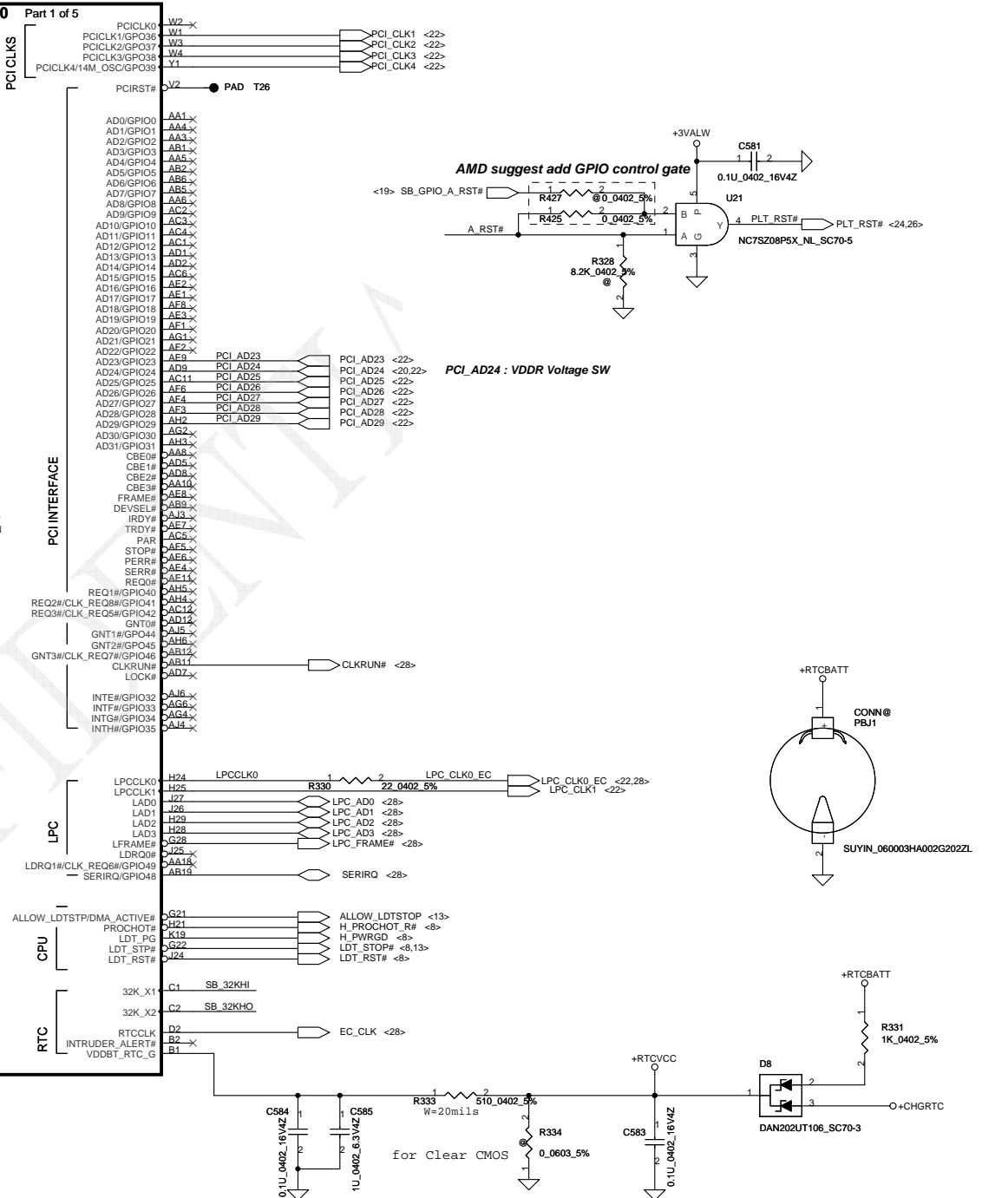
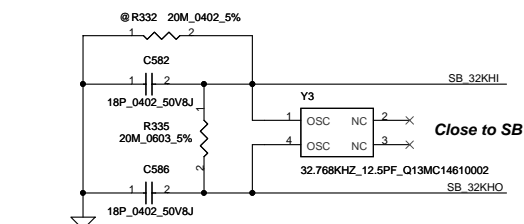
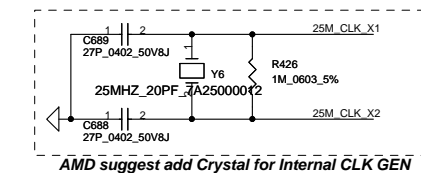


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| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc.      |                |
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|   |                    |                 |            | PEW76/86/96 LA-6552P          |                |
|   |                    |                 |            | Date: Thursday, July 22, 2010 | Sheet 17 of 45 |

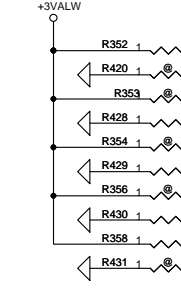
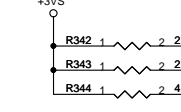
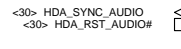
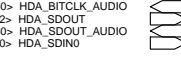
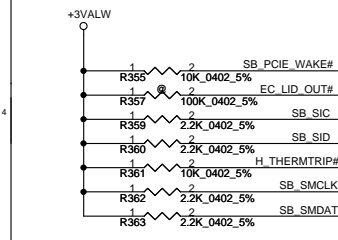
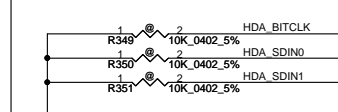
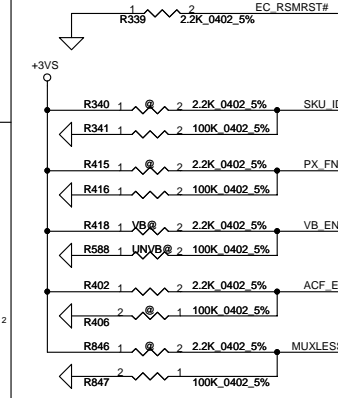
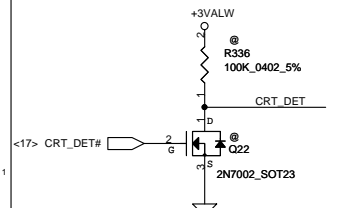


**ISL6265 PWROK input, TTL level: 0.8V~2.0V**

When this pin is high, the SVI interface is active and I2C protocol is running. While this pin is low, the SVC, SVD, and VFIXEN input states determine the pre-PWROK metal VID or VFIX mode voltage. This pin must be low prior to the ISL6265 PGOOD output going high



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|  |            |                    |            | Date: Thursday, July 22, 2010 | Sheet 18 of 45 |



Mini Card

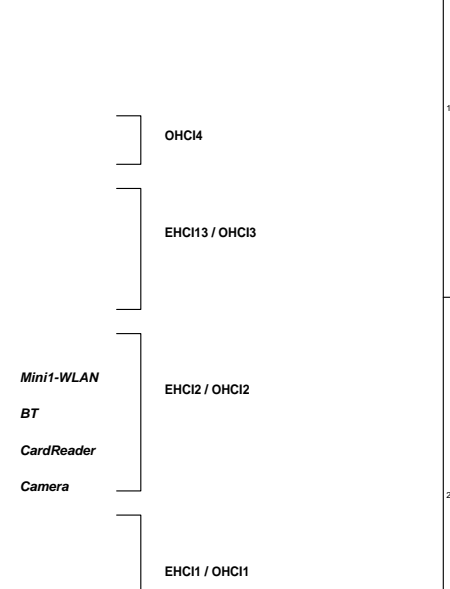
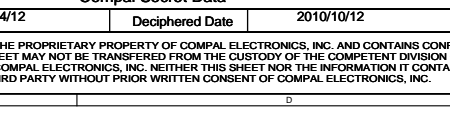
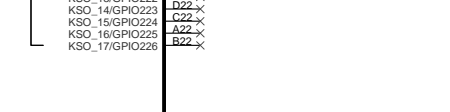
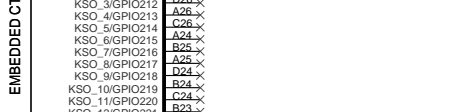
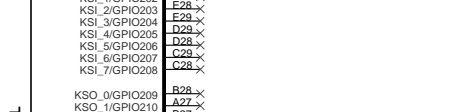
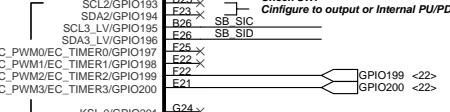
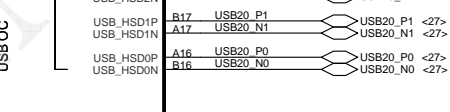
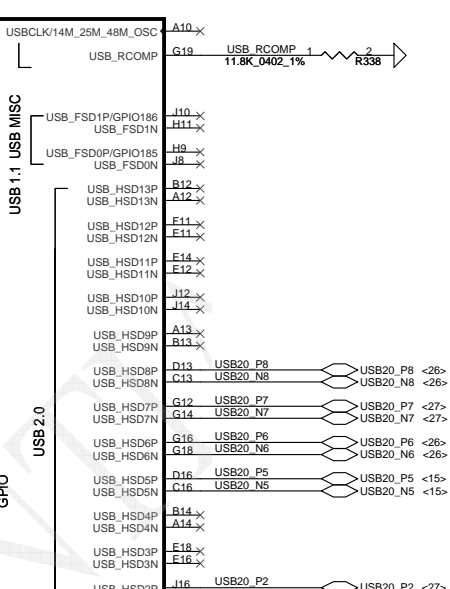
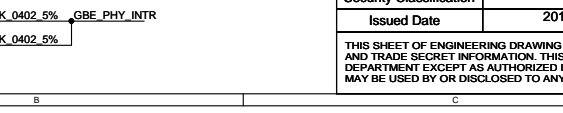
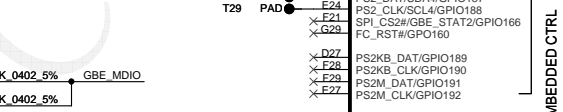
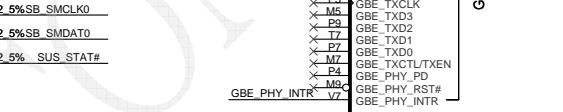
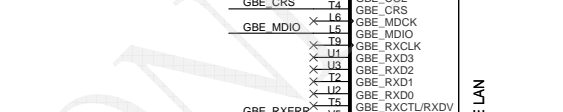
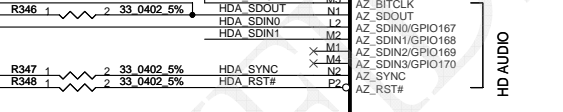
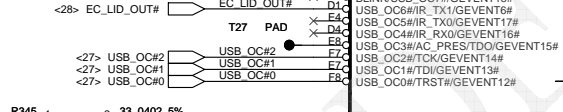
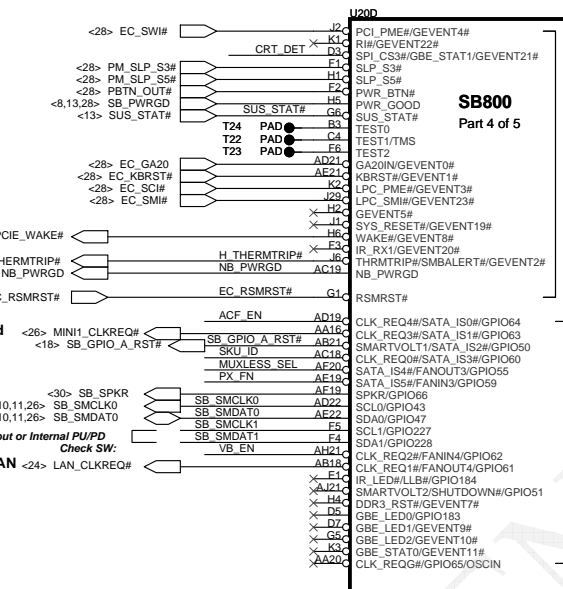
LAN

HDA

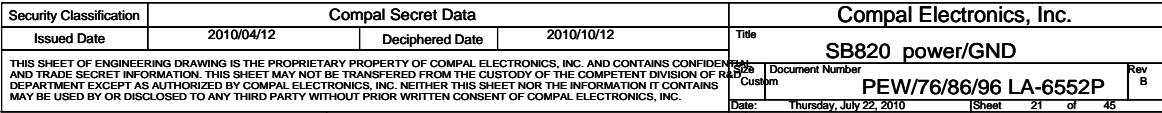
GBE

PS2

SB



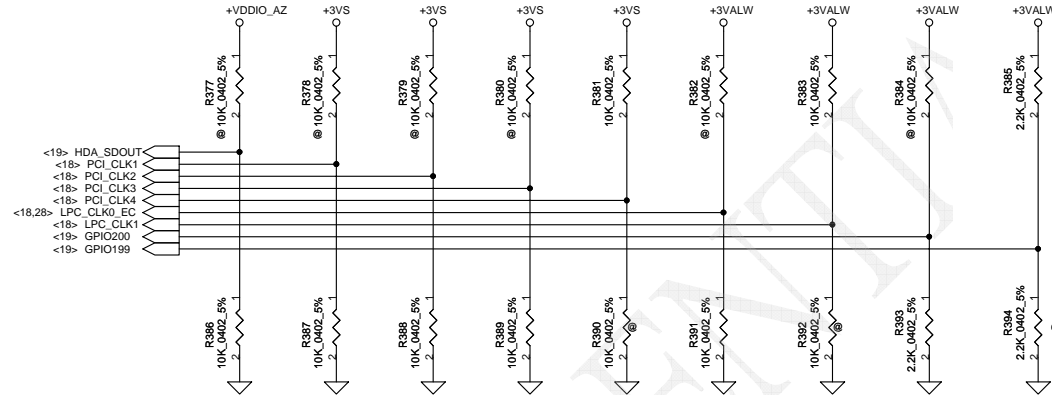




## REQUIRED STRAPS

Check Internal PU/PD

|           | AZ_SDOUT         | PCI_CLK1        | PCI_CLK2               | PCI_CLK3           | PCI_CLK4                   | LPC_CLK0   | LPC_CLK1         |  | GPIO200                                       | GPIO199 |
|-----------|------------------|-----------------|------------------------|--------------------|----------------------------|------------|------------------|--|---|---------|
| PULL HIGH | LOW POWER MODE   | ALLOW PCIE GEN2 | WATCHDOG TIMER ENABLE  | USE DEBUG STRAP    | Inter CLK Gen Mode Enable  | EC ENABLE  | CLOCKGEN ENABLE  |  | H,H = Reserved<br>H,L = SPI ROM               |         |
| PULL LOW  | Performance MODE | FORCE PCIE GEN1 | WATCHDOG TIMER DISABLE | IGNORE DEBUG STRAP | Inter CLK Gen Mode Disable | EC DISABLE | CLOCKGEN DISABLE |  | L,H = LPC ROM (Default L,NC)<br>L,L = FWH ROM |         |
|           | DEFAULT          | DEFAULT         | DEFAULT                | DEFAULT            | DEFAULT                    | DEFAULT    | DEFAULT          |  |   |         |



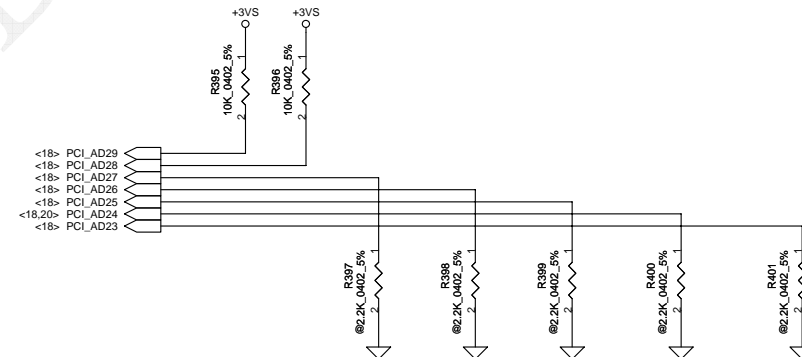
## DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

|           |  | PCI_AD27                   | PCI_AD26                           | PCI_AD25                  | PCI_AD24                               | PCI_AD23                            |
|-----------|--|----------------------------|------------------------------------|---------------------------|--|-------------------------------------|
| PULL HIGH |  | USE PCI PLL<br><br>DEFAULT | DISABLE ILA AUTORUN<br><br>DEFAULT | USE FC PLL<br><br>DEFAULT | USE DEFAULT PCIE STRAPS<br><br>DEFAULT | DISABLE PCI MEM BOOT<br><br>DEFAULT |
| PULL LOW  |  | BYPASS PCI PLL             | ENABLE ILA AUTORUN                 | BYPASS FC PLL             | USE EEPROM PCIE STRAPS                 | ENABLE PCI MEM BOOT                 |

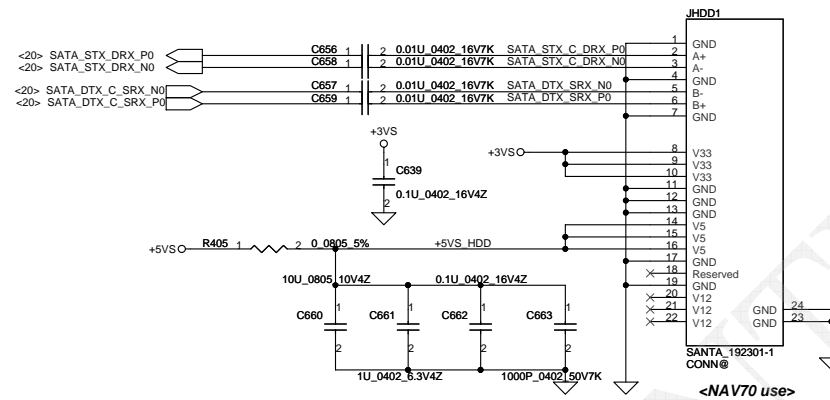
Check AD29,AD28 strap function

check default

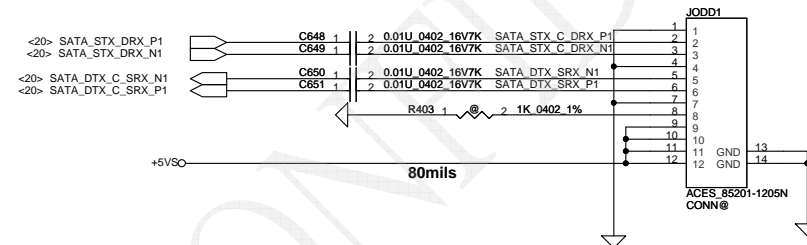


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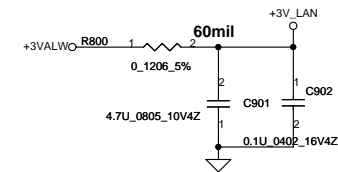
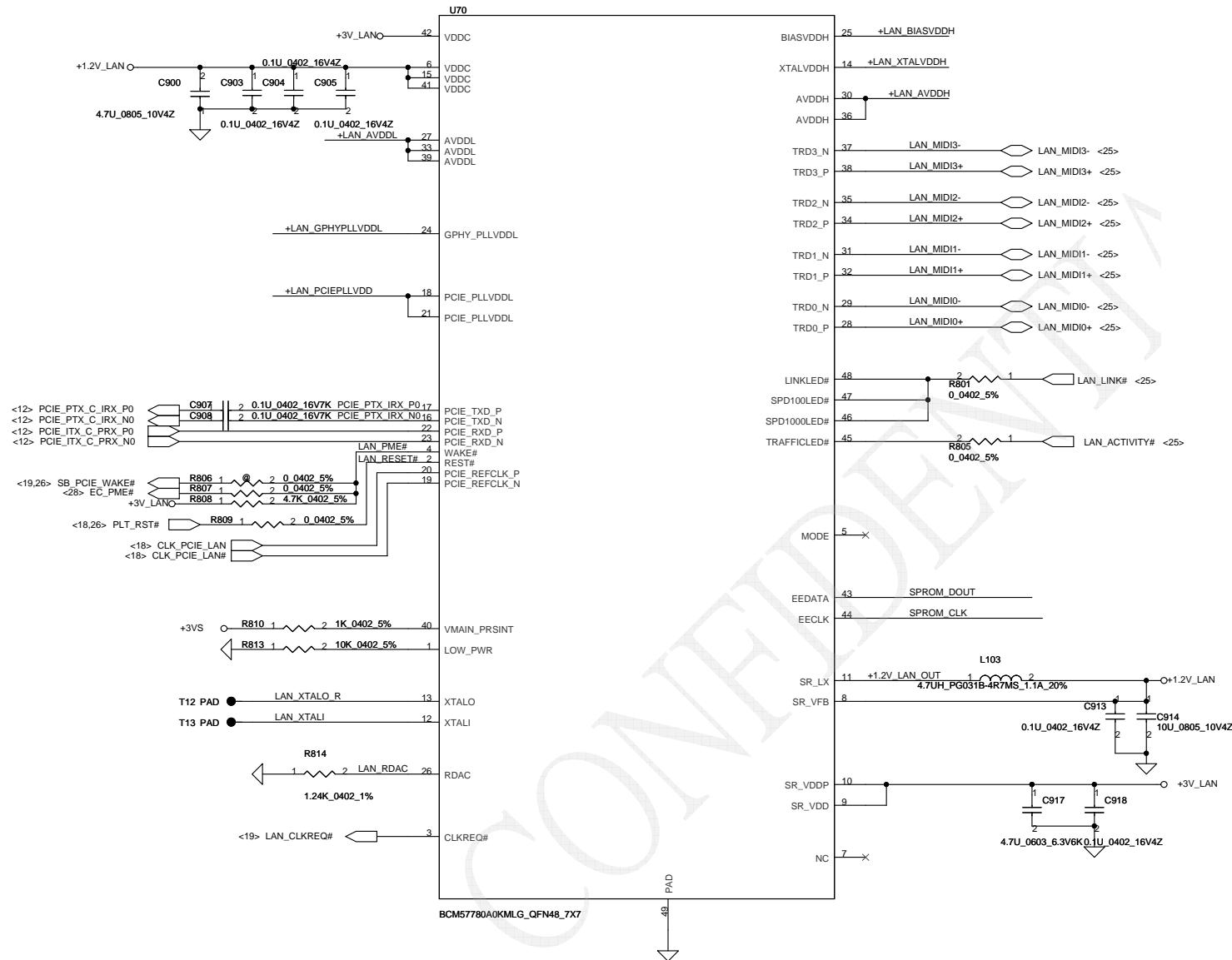
## SATA HDD Conn.



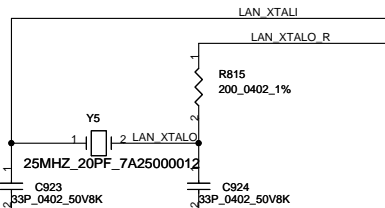
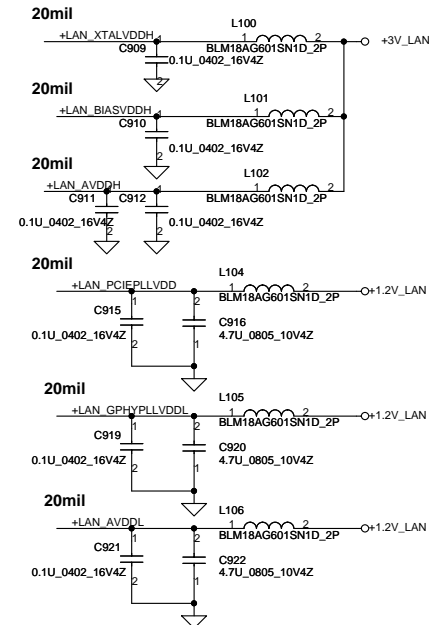
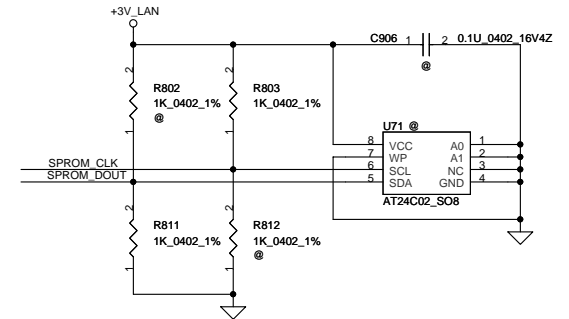
## SATA ODD FFC Conn.



|   |  |                    |  |                 |  |                          |  |                     |  |
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|   |  |                    |  |                 |  |                          |  | Document Number     |  |
| Date: Thursday, July 22, 2010   |  |                    |  | Sheet 23 of 45  |  |                          |  |                     |  |



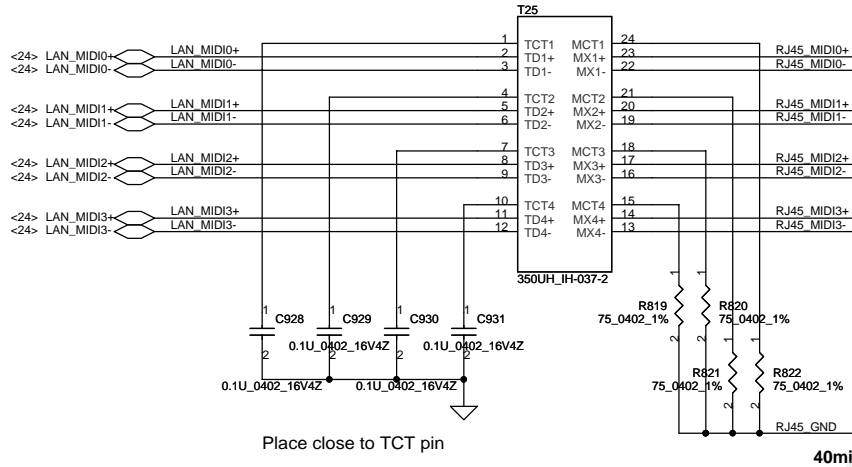
|         | SPROM_CLK<br>(EECLK) | SPROM_DOUT<br>(EEDATA) |
|---------|----------------------|------------------------|
| On chip | 1                    | 0                      |
| AT24C02 | 1                    | 1                      |



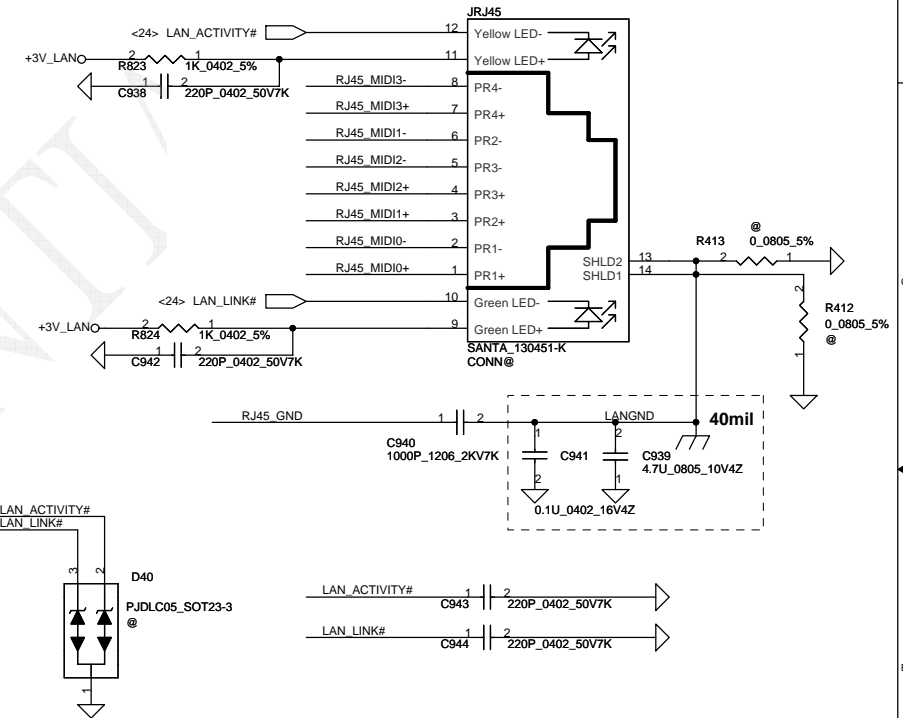
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|   |            |                    |            | Date                     | Thursday, July 22, 2010 |
|   |            |                    |            | Sheet                    | 24 of 45                |



BH GS5009-D <SP050006B00>

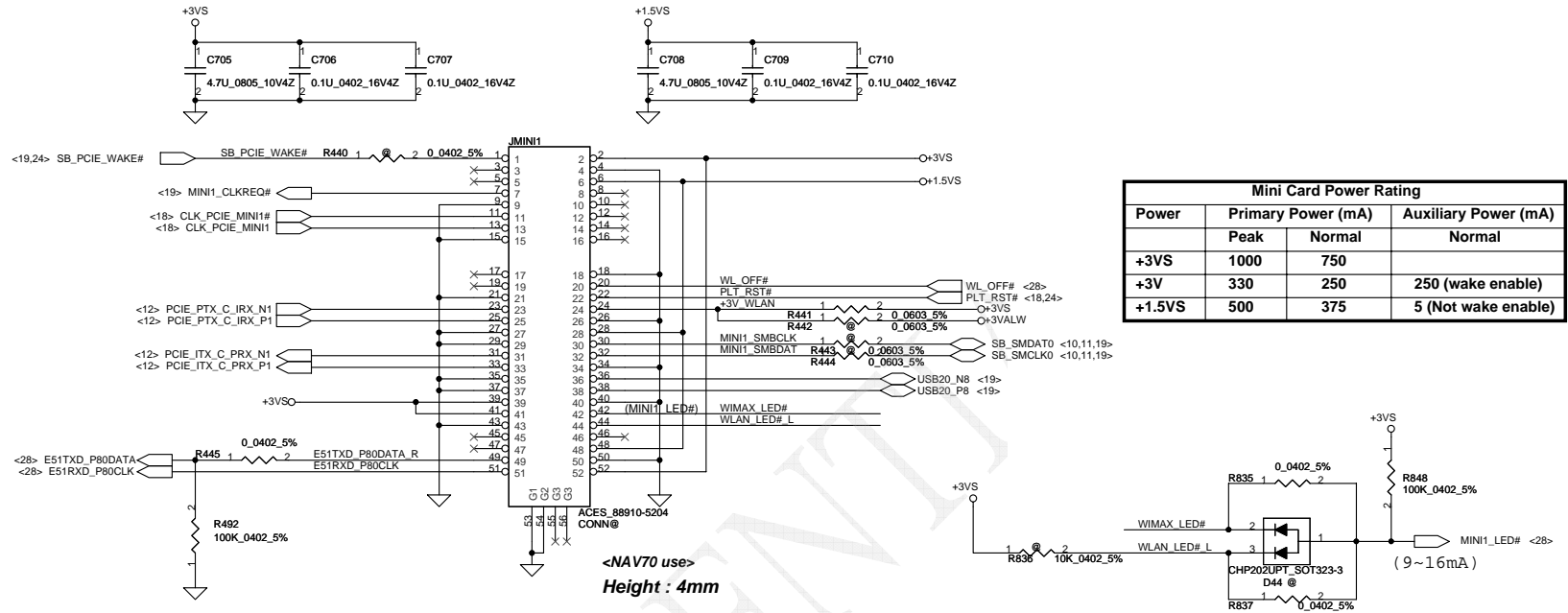


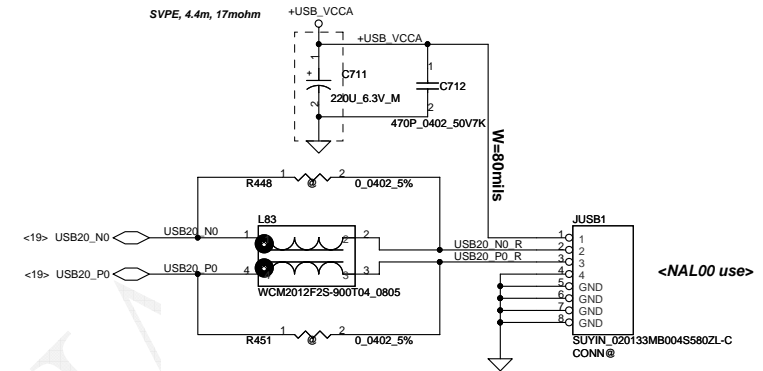
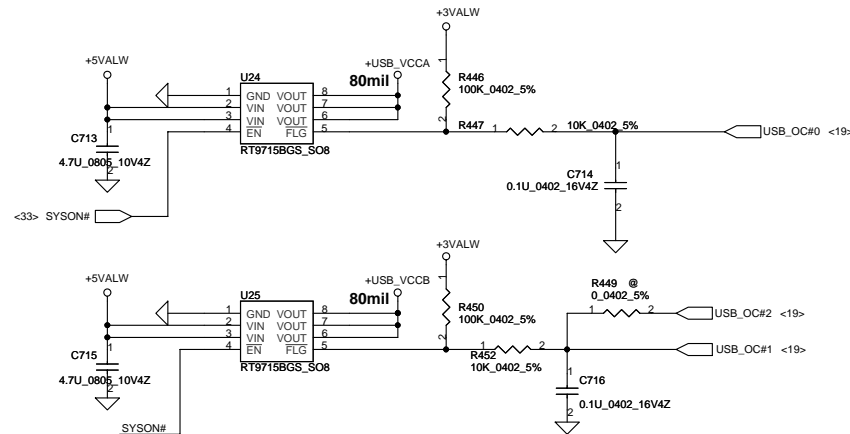
## LAN Connector



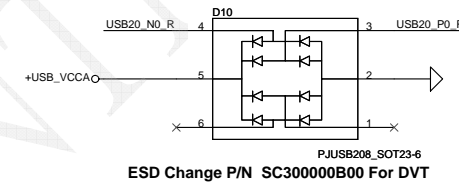
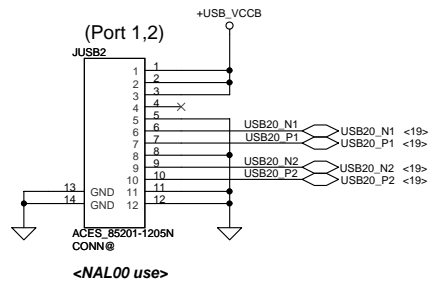
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| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc.      |                |
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|   |            |                    |            | Date: Thursday, July 22, 2010 | Sheet 25 of 45 |

## Mini-Express Card for WLAN

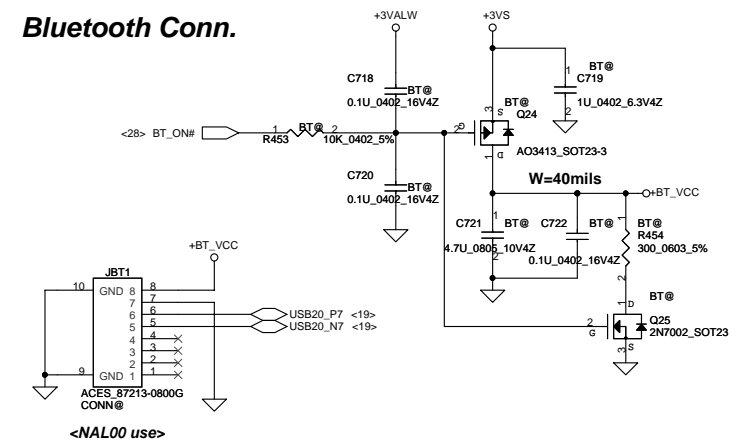




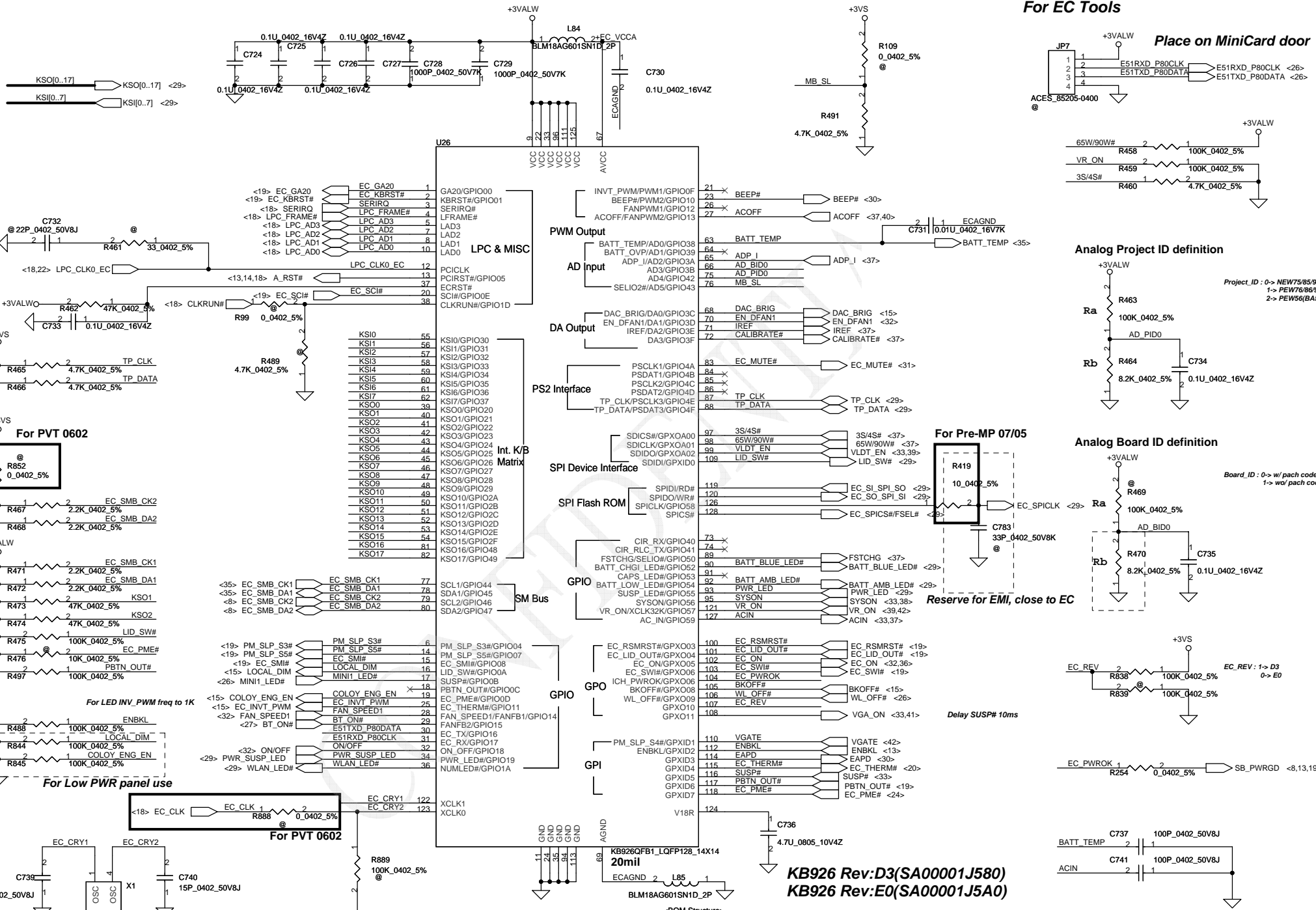
## To USB/B Connector



## Bluetooth Conn.

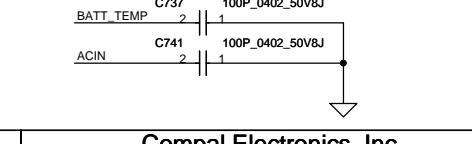
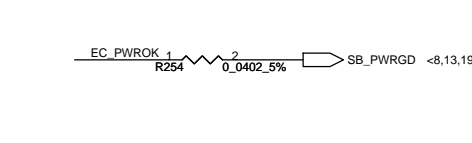
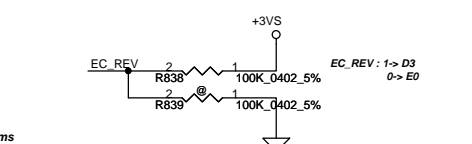
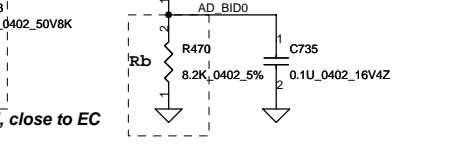
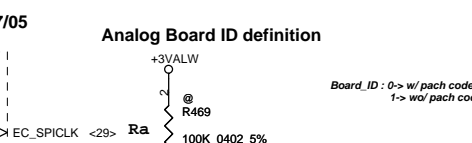
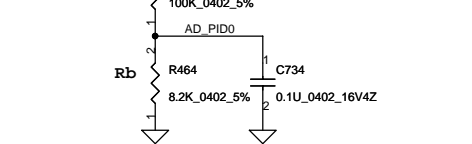
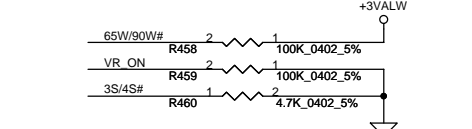
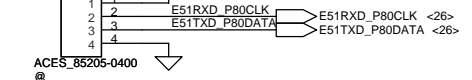


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|  |                    |                 |            | PEW76/86/96 LA-6552P          |                |
|  |                    |                 |            | Date: Thursday, July 22, 2010 | Sheet 27 of 45 |



For EC Tools

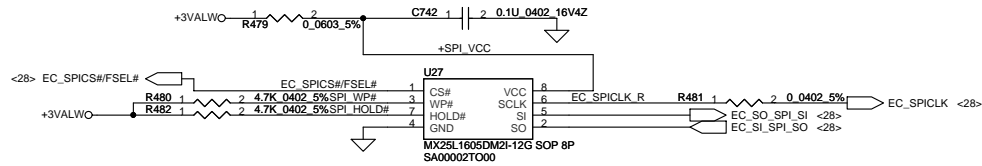
Place on MiniCard door



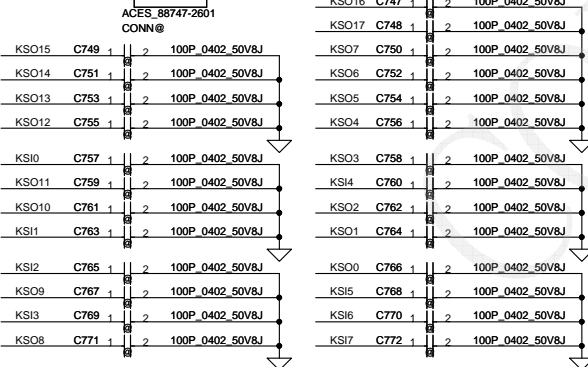
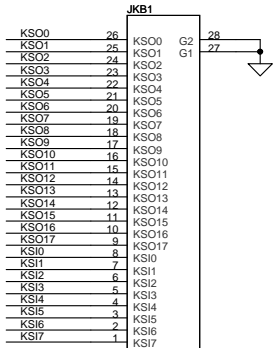
KB926 Rev:D3(SA00001J580)  
KB926 Rev:E0(SA00001J5A0)

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|   |            | PEW/76/86/96 LA-6552P   |            |                          |       |
| Date  |            | Thursday, July 22, 2010 | Sheet      | 28                       | of 45 |

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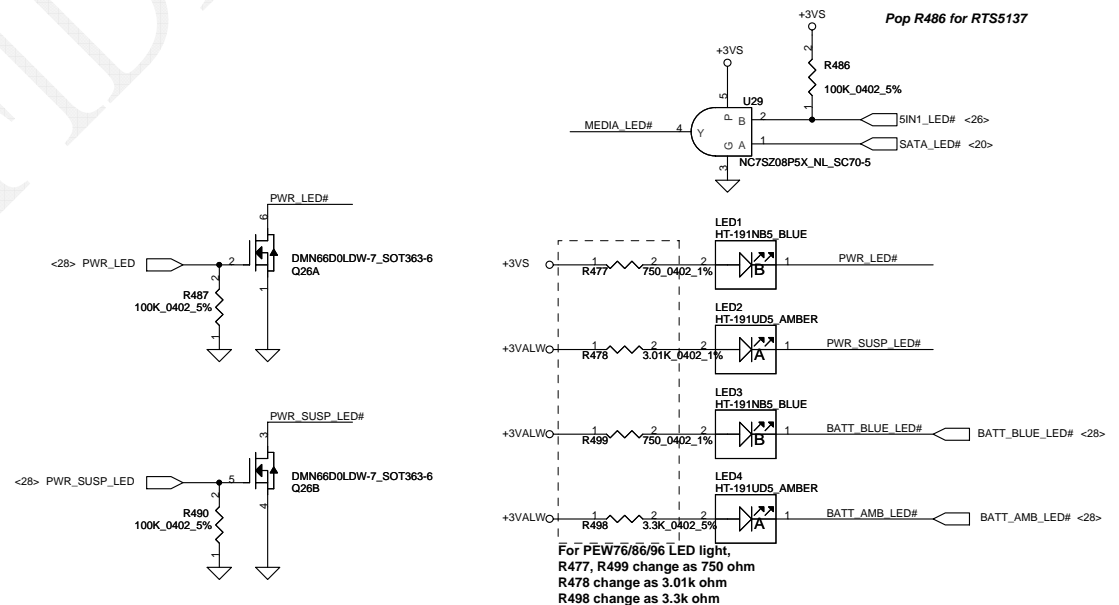
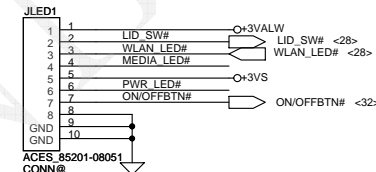
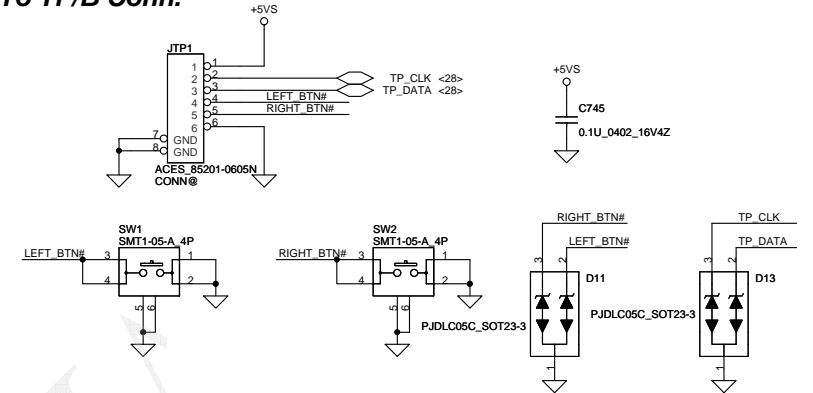


### INT\_KBD Conn.



For PVT 0608 Unpop Cap.

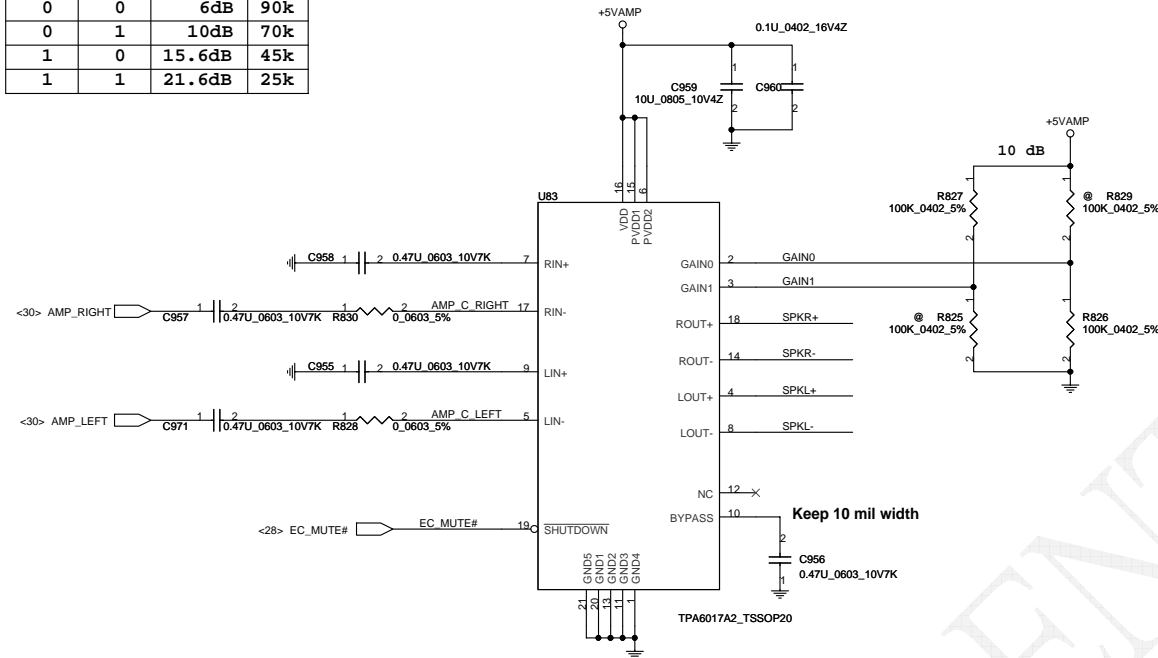
### To TP/B Conn.



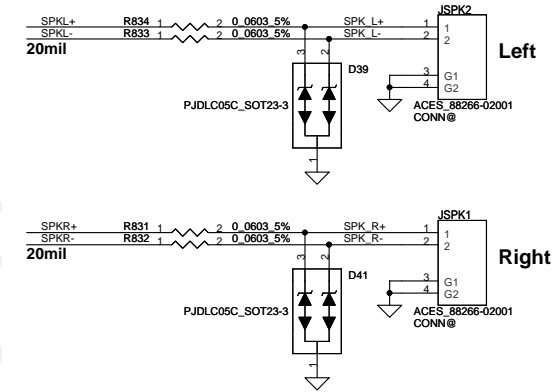
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| Security Classification   |            | Compal Secret Data      |            | Compal Electronics, Inc. |                                |
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| Document Number   |            |                         |            | PEW/76/86/96 LA-6552P    | Rev B                          |
| Date:   |            | Thursday, July 22, 2010 |            | Sheet                    | 29 of 45                       |



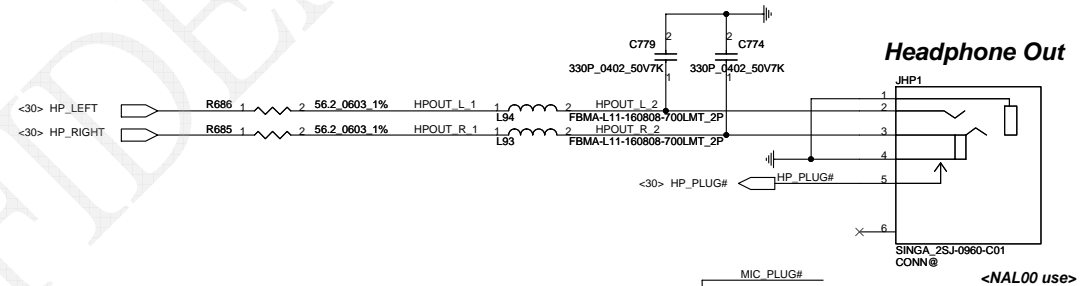
| GAIN0 | GAIN1 | AV(inv) | Ri  |
|-------|-------|---------|-----|
| 0     | 0     | 6dB     | 90k |
| 0     | 1     | 10dB    | 70k |
| 1     | 0     | 15.6dB  | 45k |
| 1     | 1     | 21.6dB  | 25k |



### Int. Speaker Conn.

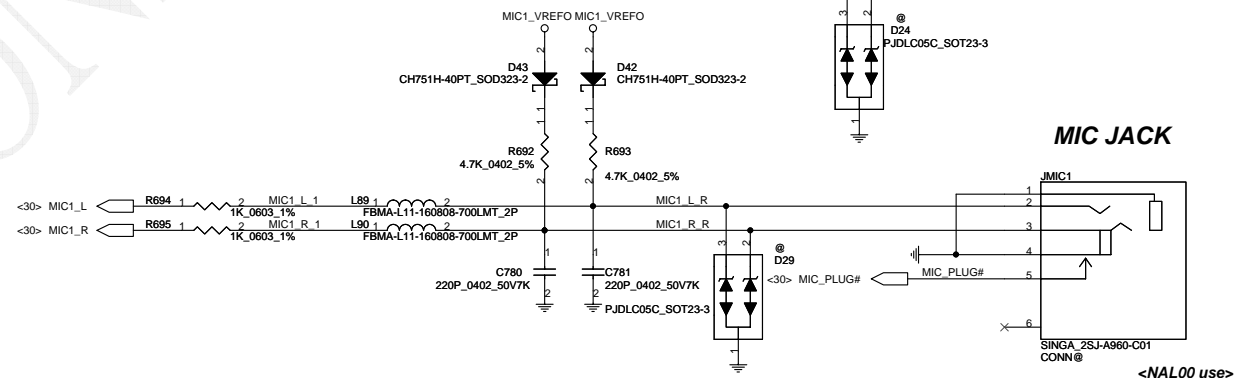


### Headphone Out



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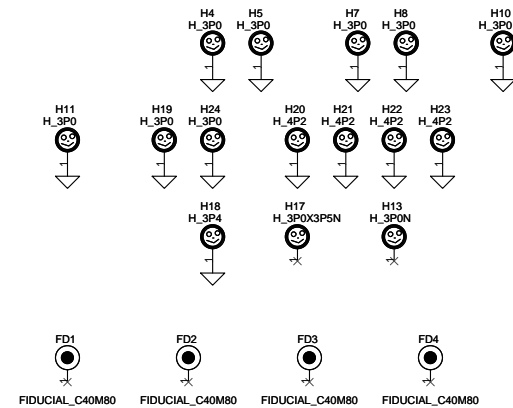
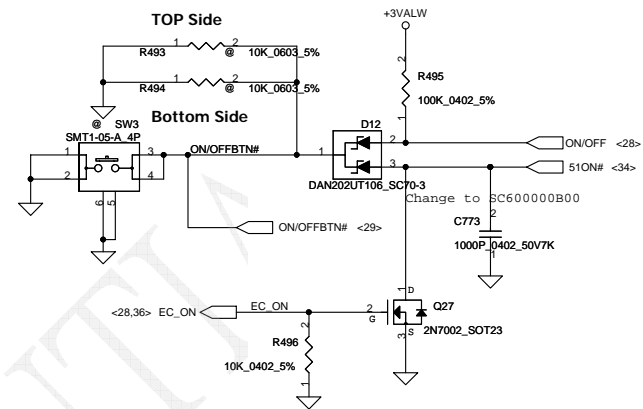
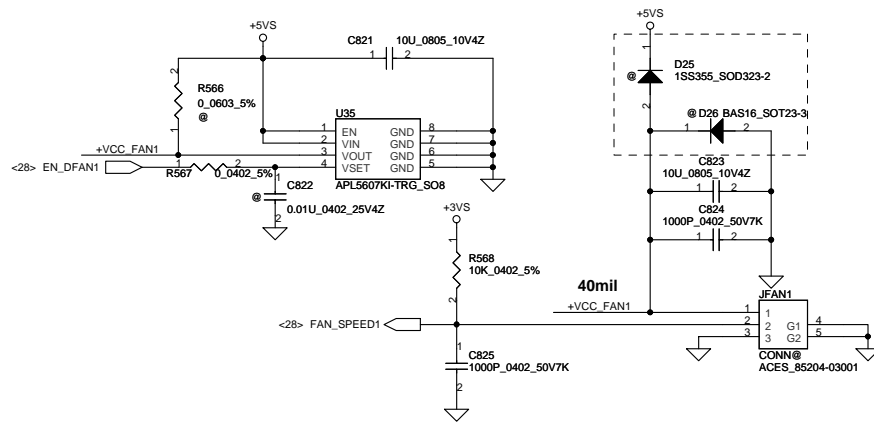
### MIC JACK



<NAL00 use>

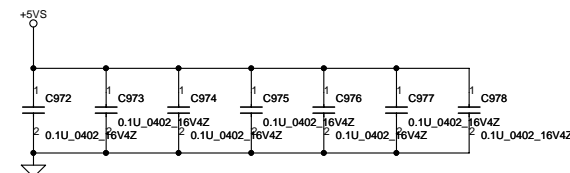
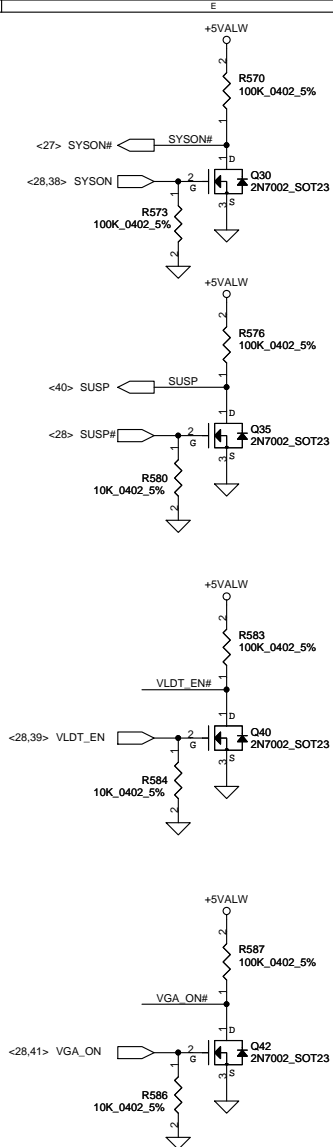
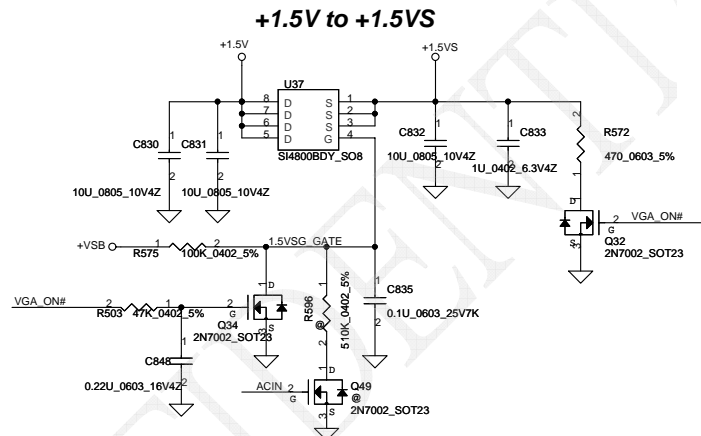
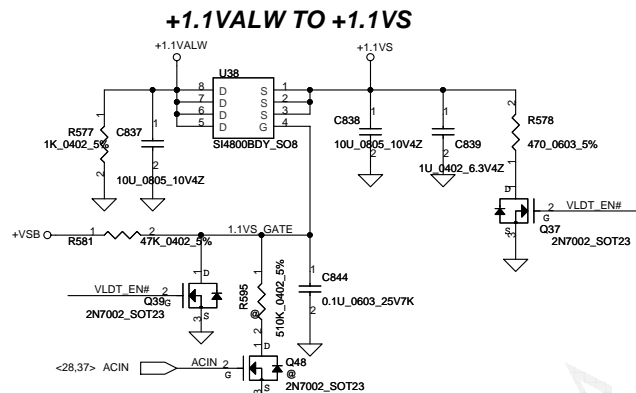
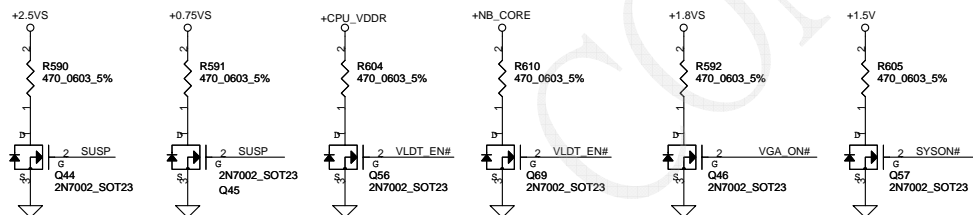
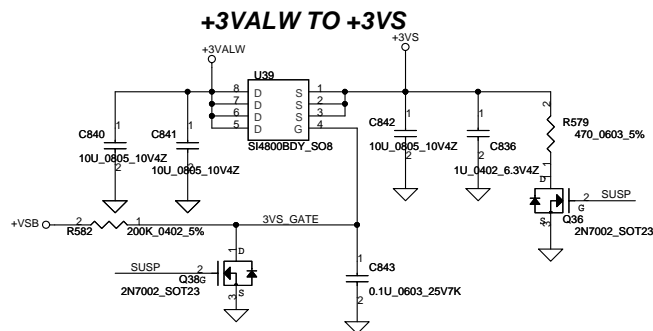
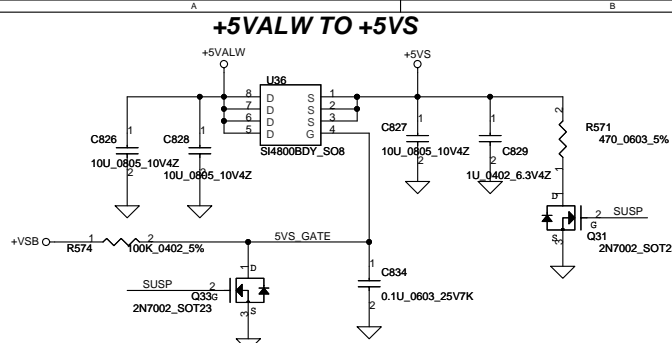
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|---|--|--------------------|--|-----------------|--|--------------------------|--|-------------------------------|--|-----------------------|--|-------|--|
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|   |  |                    |  |                 |  |                          |  | Date: Thursday, July 22, 2010 |  | Sheet 31 of 45        |  |       |  |
|   |  |                    |  |                 |  |                          |  |                               |  |                       |  |       |  |

ON/OFF switch **Power Button**



|   |                    |                 |            |                          |       |  |
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|   |                    |                 |            | Document Number          | Rev B |  |
|   |                    |                 |            | PEW/76/86/96 LA-6552P    |       |  |
| Date: Thursday, Jul 22, 2010  |                    |                 |            | Sheet 32 of 45           |       |  |

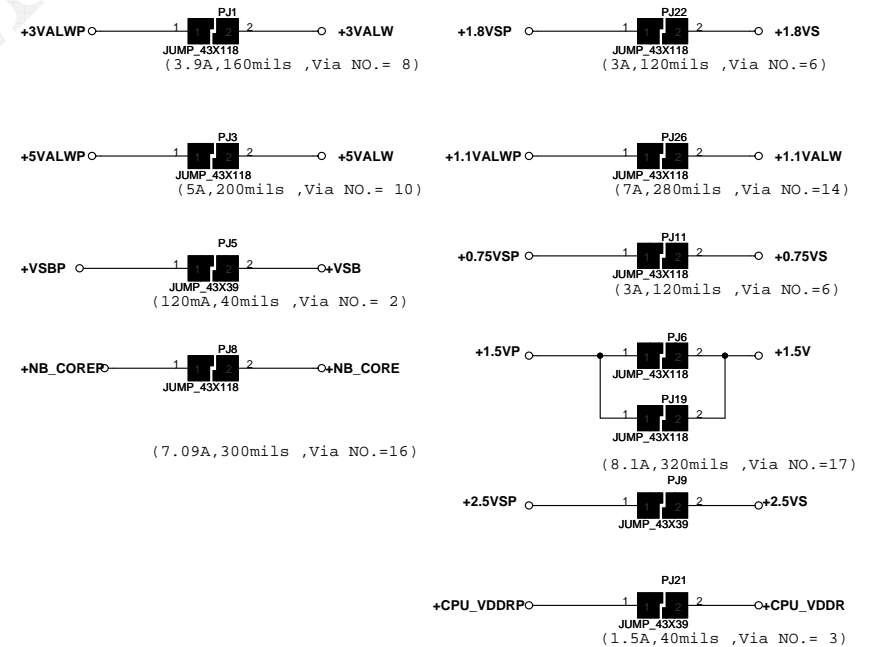
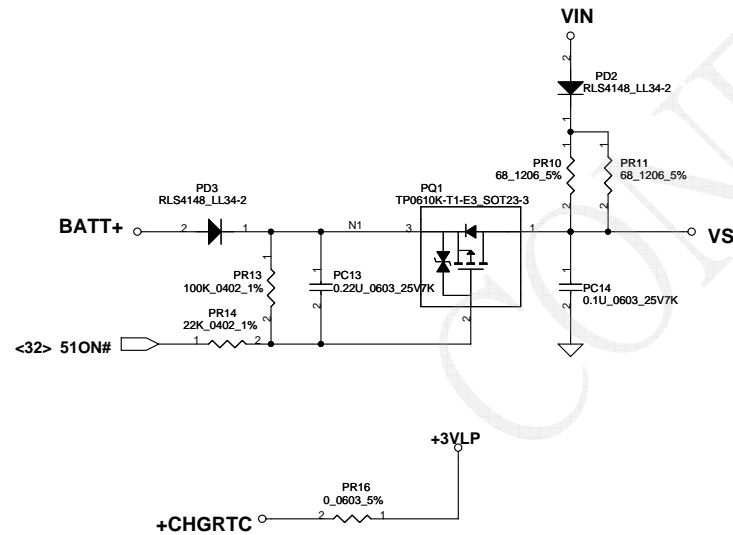
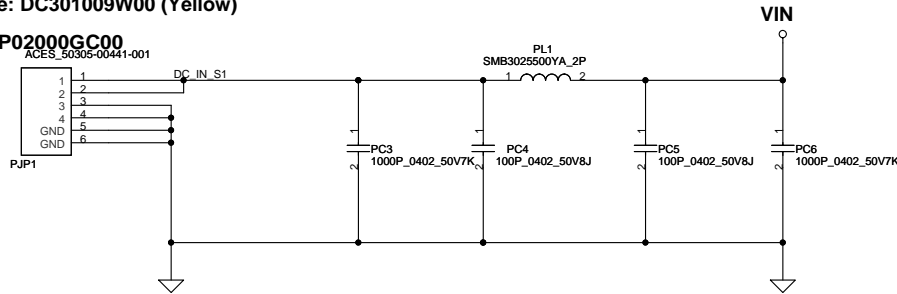




|  |            |                    |            |                               |                |
|--|------------|--------------------|------------|-------------------------------|----------------|
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|  |            |                    |            | PEW/76/86/96 LA-6552P         |                |
|  |            |                    |            | Date: Thursday, July 22, 2010 | Sheet 33 of 45 |

DC-IN cable: DC301009W00 (Yellow)

SP02000GC00  
ACES\_90305-00441-001

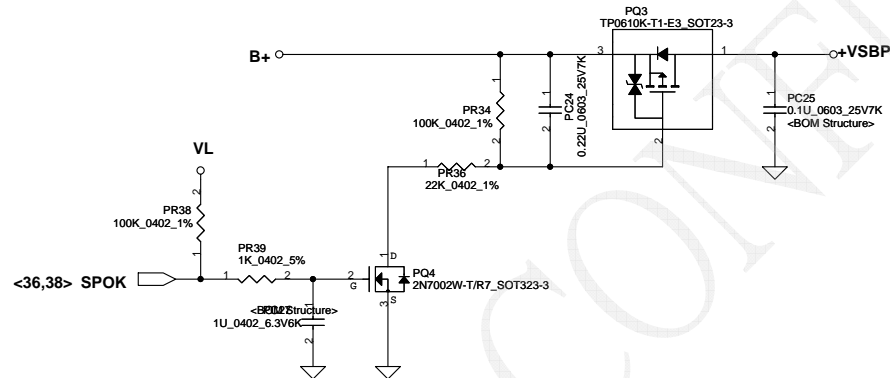
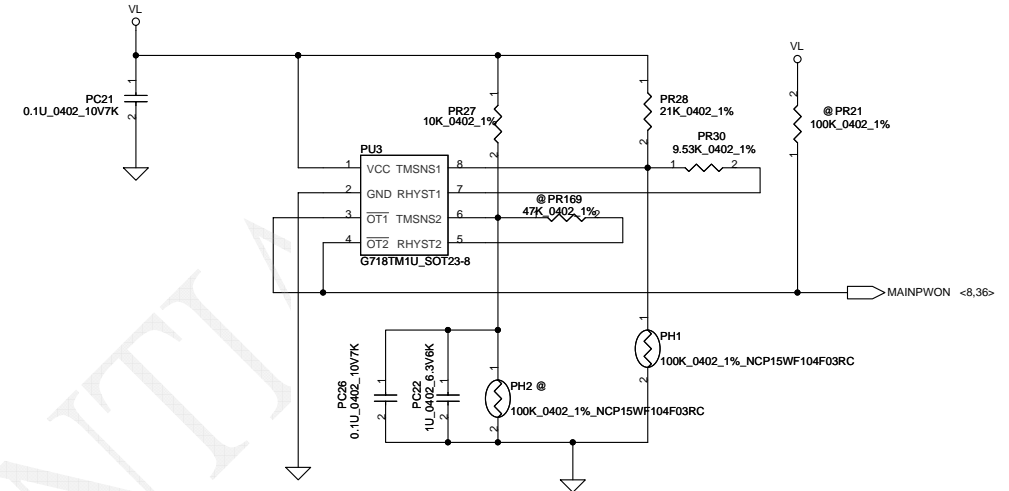
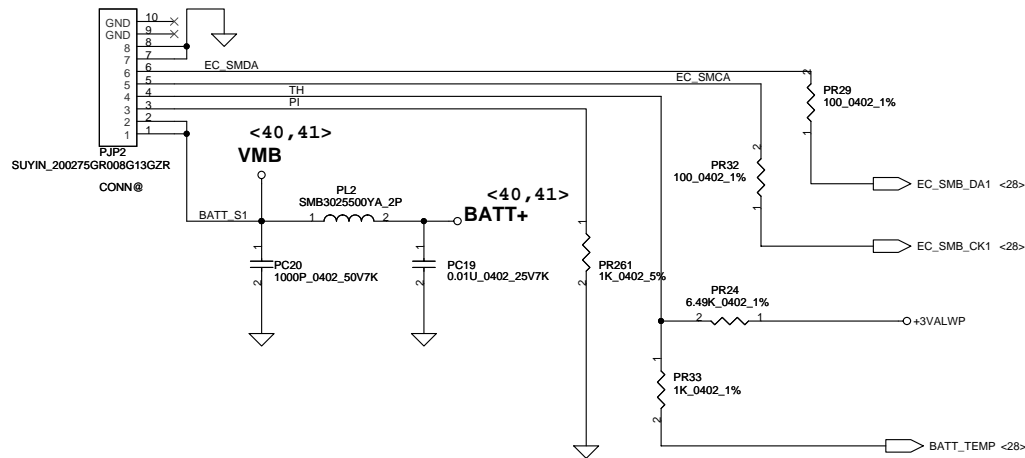


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|   |            |                    |            | PEW96 LA-6552P           | B   |
| Date: Thursday, July 22, 2010   |            |                    |            | Sheet                    | 45  |

PH1 under CPU bottom side : Not SPEC, reference only

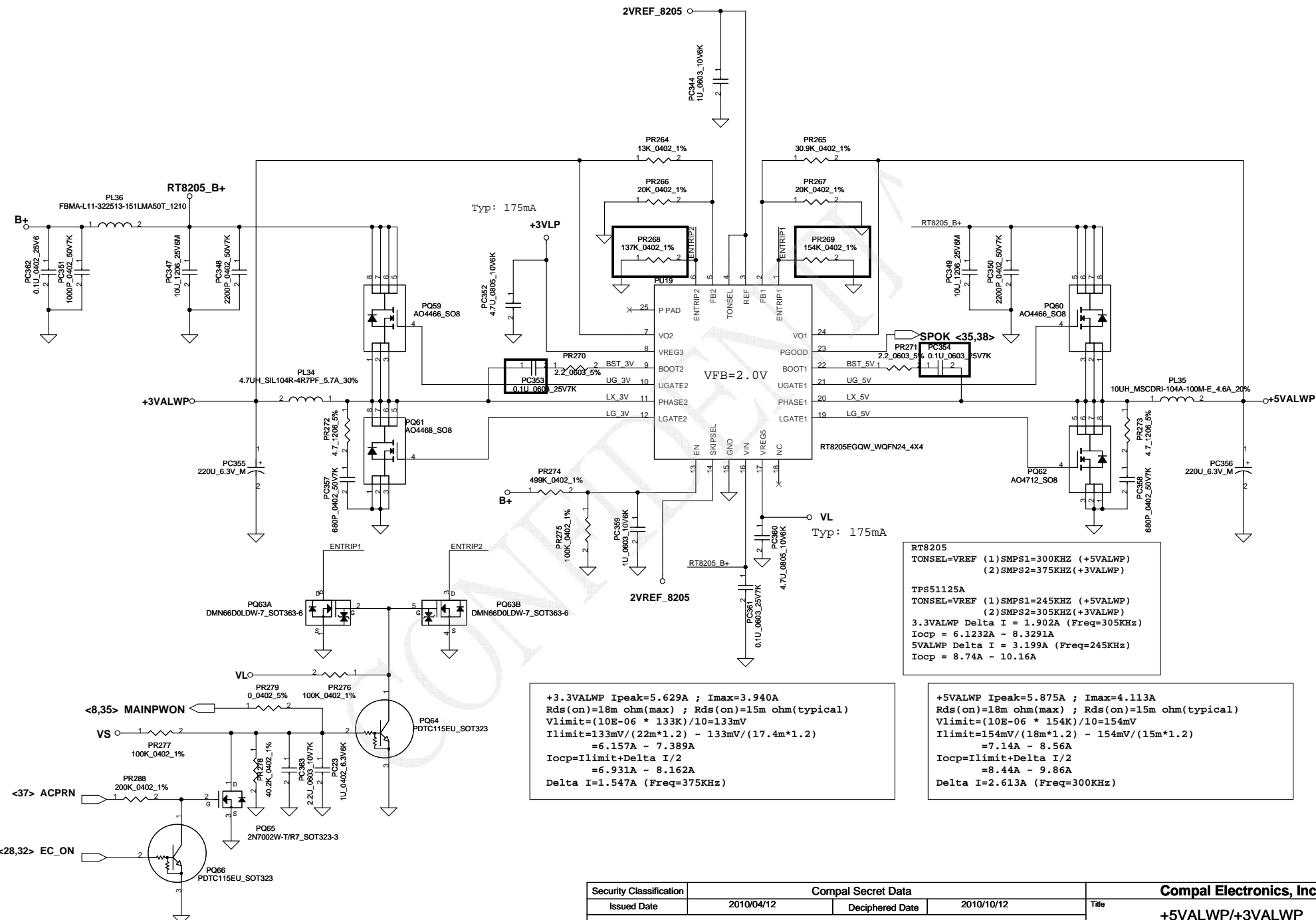
CPU thermal protection at 92 degree C

Recovery at 56 degree C



|   |                    |                 |            |                               |                |
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|   |                    |                 |            | PEW96 LA-6552P                |                |
|   |                    |                 |            | Date: Thursday, July 22, 2010 | Sheet 35 of 45 |

Note:  
Use TPS51125 IC can remove RTC refernece LDO  
Use TPS51427 IC must keep RTC refernece LDO

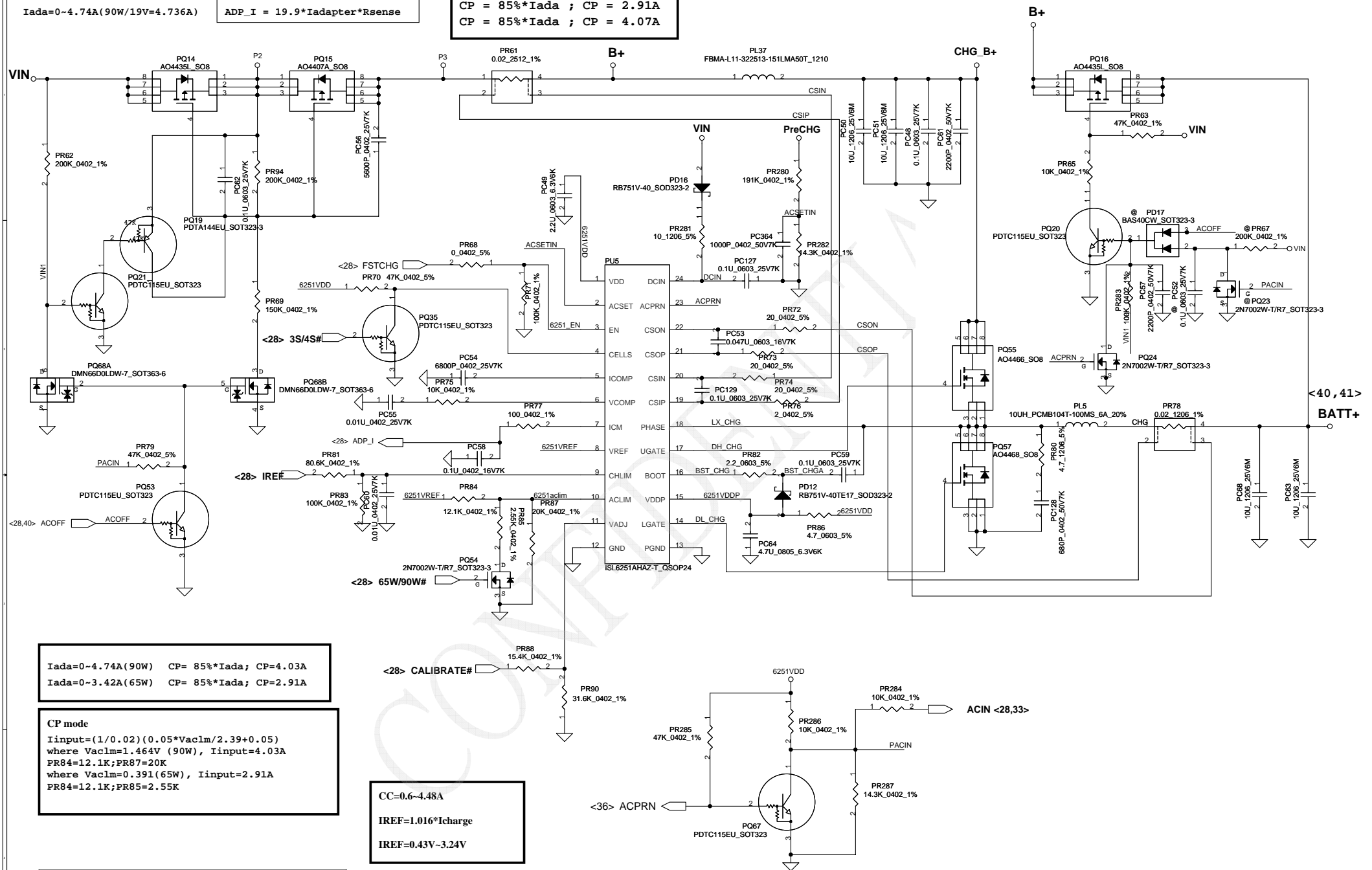


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|   |  |                    |  |                 |  |                          |  | +5VALWP/+3VALWP |  |
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|   |  |                    |  |                 |  | Rev B                    |  |                 |  |
| Date:   |  |                    |  |                 |  | Thursday, July 22, 2010  |  | Sheet 36 of 45  |  |

$I_{ada}=0\sim 4.74A(90W/19V=4.736A)$

$$ADP\_I = 19.9 \cdot I_{\text{adapter}} \cdot R_{\text{sense}}$$

CP = 85%\*Iada ; CP = 2.91A  
CP = 85%\*Iada ; CP = 4.07A



**I<sub>ada</sub>=0~3.42A (65W)    CP= 85%\*I<sub>ada</sub>; CP=2.91A**

```
Iinput=(1/0.02)*(0.05*Vac1m/2.39+0.05)
where Vac1m=1.464V (90W), Iinput=4.03A
PR84=12.1K;PR87=20K
where Vac1m=0.391(65W), Iinput=2.91A
PR84=12.1K;PR85=2.55K
```

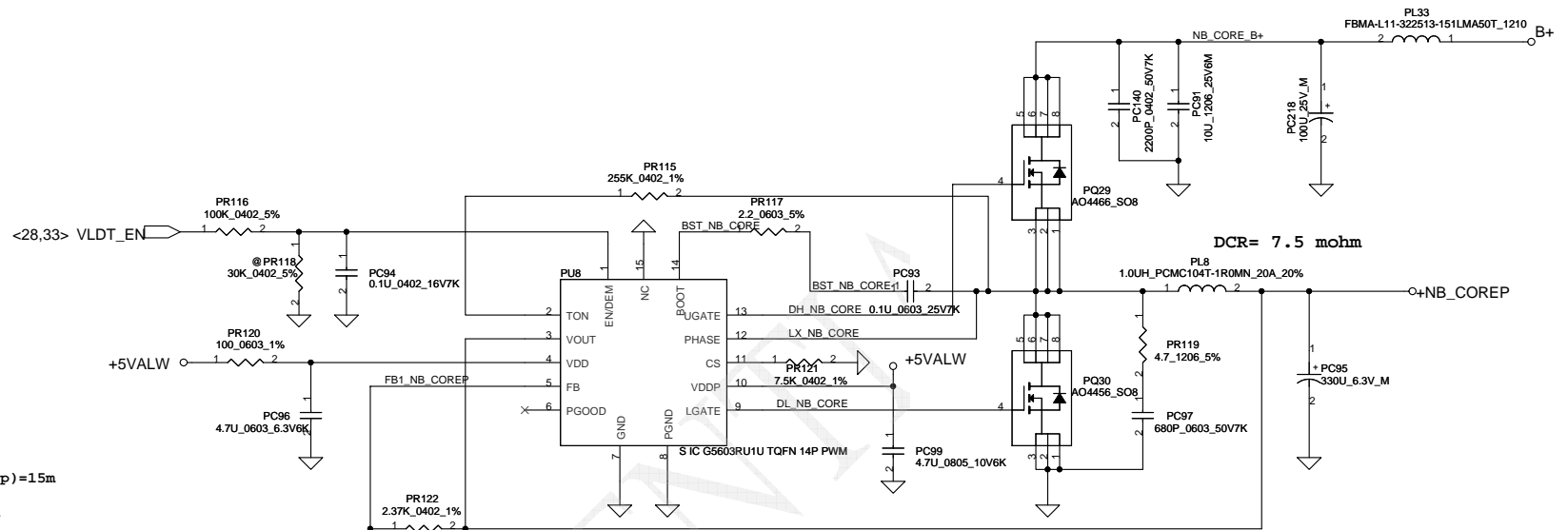
**IREF=0.43V~3.24V**

| BATT Type             | Charging Voltage<br>(0x15) | CV mode |
|-----------------------|----------------------------|---------|
| Normal 3S LI-ON Cells | 12600mV                    | 12.60V  |

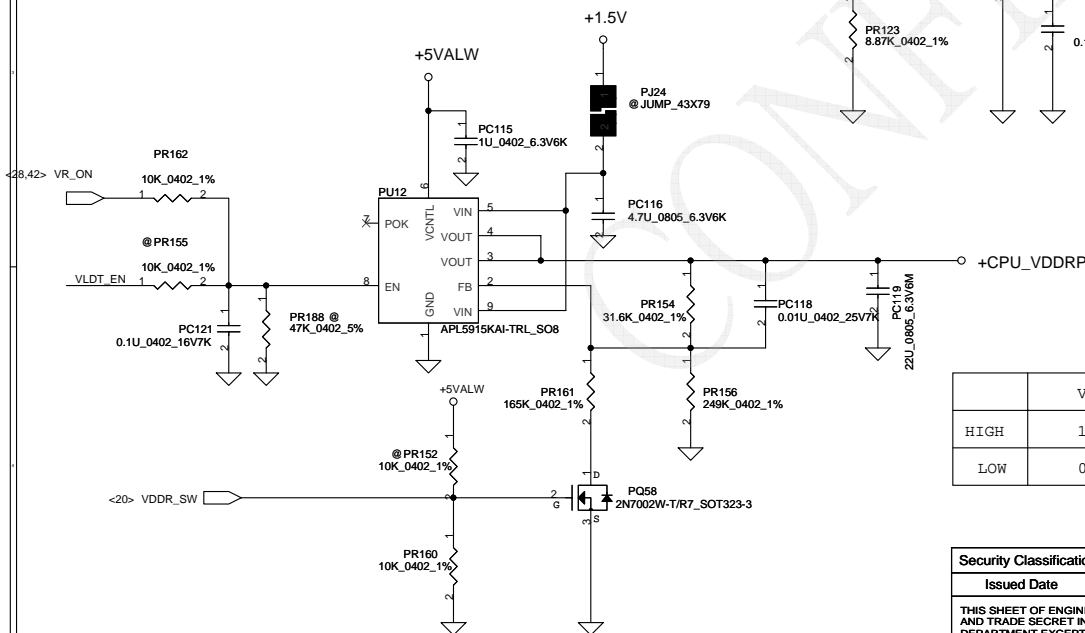
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| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc.      |                 |
| Issued Date   | 2010/04/12 | Deciphered Date    | 2010/10/12 | Title                         | CHARGER         |
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|   |            |                    |            | Date: Thursday, July 22, 2010 | Rev B           |
|   |            |                    |            | Sheet 37 of 45                |                 |



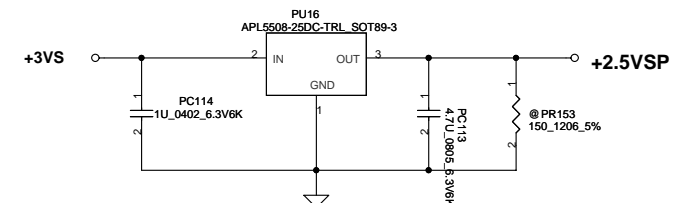
$<V_o=1.1V>$   $V_{FB}=0.75V$   
 $V=0.75*(1+4.7K/10K)=1.1V$   
 $F_{sw}=280KHz$   
 $C_{out} ESR=15m\ ohm$   $R_{dson(max)}=18m$   $R_{dson(typ)}=15m$   
 $I_{peak}=7.6A$ ,  $I_{max}=5.4A$ ,  $I_{ocp}=9.2A$   
 $\Delta I=((19-1.1)*(1.1/19))/(L*F_{sw})=2.06A$   
 $\Rightarrow 1/2\Delta I=1.03A$   
 $V_{tripmax}=I_{ocp}*R_{dson}=9.2*5.6*1.3=0.067V$   
 $R_{cs}=V_{trip}/9\mu A=0.067V/9\mu A=7.44K$   
 choose  $R_{cs}=7.5K$   
 $I_{ocpmax}=(7.5K*11\mu A)/(0.0045)+1.03A=19.36A$   
 $I_{ocpmin}=(7.5K*9\mu A)/(0.018*1.3)+1.03A=10.3A$   
 $I_{ocp}=10.3A\sim 19.36A$

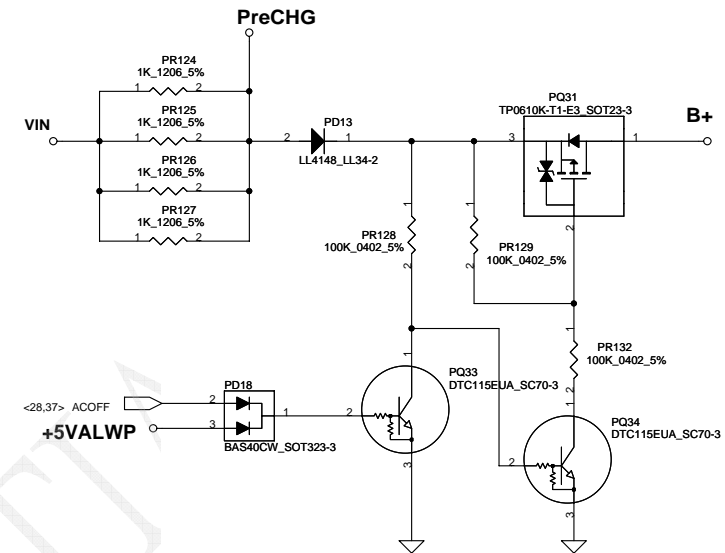
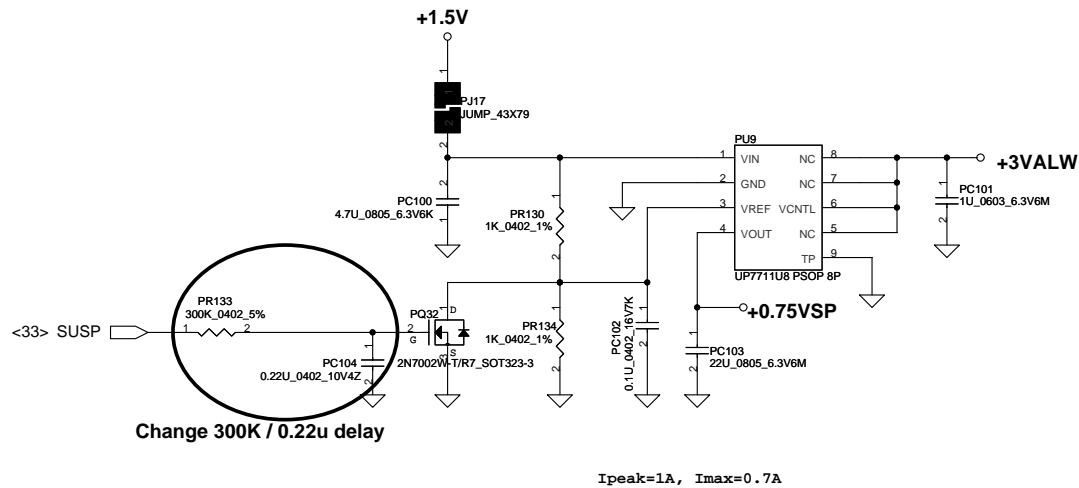


|      | POWER_SEL |
|------|-----------|
| HIGH | 0.95V     |
| LOW  | 1.1V      |



|      | VDDR_SW |
|------|---------|
| HIGH | 1.05V   |
| LOW  | 0.9V    |





|   |            |                    |            |                          |                         |
|---|------------|--------------------|------------|--------------------------|-------------------------|
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|   |            |                    |            | Date:                    | Thursday, July 22, 2010 |
|   |            |                    |            | Sheet                    | 40 of 45                |







| Item | Fixed Issue                    | Reason for change  | Rev. | PG# | Modify List  | Date         | Phase  |
|------|--------------------------------|--|------|-----|--|--------------|--------|
| 1    | Modify Pre-charger             |  |      |     | Add PR279,PR288,PC57<br>Change PR285 100K to 47K<br>Change PR287 20K to 14.3K<br>Change PQ67 2N7002 to PDTCT115<br>Change PR62 47K to 200K<br>Change PR79 22K to 47K<br>Change PR283 0 to 100K | 2010<br>0528 | PVT    |
| 2    | Meet common rule               |  |      |     | Change PJ30 to PL36, PJ23 to PL37<br>Add PC361,PC362   | 2010<br>0602 | PVT    |
| 3    | HDMI test fail                 | 5V voltage too low at test termial   |      | 36  | Change PR265 from 30K to 30.9K   | 2010<br>0604 | PVT    |
| 4    | ESD test fail                  | ESD solution   |      |     | Add PC22, PC23   | 2010<br>0608 | PVT    |
| 5    | EMI test fail                  | EMI solution   |      |     | Enable 3V,5V,1.1V,1.5V,NB_CORE,CPU snubber   | 2010<br>0608 | PVT    |
| 6    | Power sequence tune            |  |      | 41  | Change PR144 from 22K to 200K<br>Change PC156 from 0.47u to 0.22u  | 2010<br>0609 | PVT    |
| 7    | Costdown                       | Costdown   |      | 38  | Change PQ28 from AO4456 to AO4712<br>Change PR112 from 13K to 18.2K<br>Change PL7 from 1.0uH to 1.8uH<br>Change PQ61 from AO4712 to AO4468   | 2010<br>0617 | PVT    |
| 8    |                                |  |      |     | PR268 from 133K to 137K<br>PQ57 from AO4466 to AO4468  |              |        |
| 9    | For DDR voltage default/HW YC  | DDR 2 need 0.9V, DDR 3 need 1.05V<br>But DDR2 voltage is critical then DDR 3 |      | 39  | Disable PR152<br>Enable PR160  | 2010<br>0705 | Pre MP |
| 10   | Aprove 200MHz~220MHz/EMI Chris | EMI solution   |      | 37  | Enable PR80, PC128<br>Change PR82 from 0 to 2.2  | 2010<br>0705 | Pre MP |
| 11   | Add a bypass path/ESD Chris    | ESD solution   |      | 35  | Add PC26 near PC22   | 2010<br>0705 | Pre MP |
| 12   |                                |  |      |     |  |              |        |
| 13   |                                |  |      |     |  |              |        |
| 14   |                                |  |      |     |  |              |        |
| 15   |                                |  |      |     |  |              |        |
| 16   |                                |  |      |     |  |              |        |

|   |            |                    |            |                               |  |
|---|------------|--------------------|------------|-------------------------------|--|
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| PEW96 LA-6552P  |            |                    |            | Date: Thursday, July 22, 2010 |  |
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| Item | Fixed Issue | Reason for change | Rev. | PG# | Modify List | Date | Phase |
|------|-------------|-------------------|------|-----|-------------|------|-------|
| 1    |             |                   |      |     |             |      |       |
| 2    |             |                   |      |     |             |      |       |
| 3    |             |                   |      |     |             |      |       |
| 4    |             |                   |      |     |             |      |       |
| 5    |             |                   |      |     |             |      |       |
| 6    |             |                   |      |     |             |      |       |
| 7    |             |                   |      |     |             |      |       |
| 8    |             |                   |      |     |             |      |       |
| 9    |             |                   |      |     |             |      |       |
| 10   |             |                   |      |     |             |      |       |
| 11   |             |                   |      |     |             |      |       |
| 12   |             |                   |      |     |             |      |       |
| 13   |             |                   |      |     |             |      |       |
| 14   |             |                   |      |     |             |      |       |
| 15   |             |                   |      |     |             |      |       |
| 16   |             |                   |      |     |             |      |       |

|   |                    |                 |                          |                |
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05/10 First release

- 1. Change Cardreader chip (RTS5137/RTS5138)
- 2. ODD used to ODD sub/b
- 3. RTC Battery change (w/o charge)

06/11 PVT

- 1. P.28 Reserve R889 For EC\_CLK, pop R851, unpop R852 For EC\_SMBus leakage
- 2. P.26 Remove R853
- 3. P.28 project ID-->1 Board ID -->1, unstuff KSI, KSO Cap.
- 4. P.8 Change R41 as 31.6k ohm and R42 as 30k ohm for TSI

07/05 Pre-MP

- 1. P.19 Reserve R890 For MEM\_1V5
- 2. P.28 Change R419 as 10 ohm For EMI

07/20

- 1. P.29 Change R477, R499 as 750 ohm; change R478 as 3.01k ohm; change R498 as 3.3k ohm for LED light

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